

Compal Confidential

EH7LW/EH5LW/FH5TW/EH7LC/EH5LC

DIS MB Schematic Document

LA-H791P

Rev: 2.0

2019.05.29

Security Classification		Compal Secret Data		Title	
Issued Date		2018/12/27	Deciphered Date	2019/12/27	2019/12/27
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HDMI Conn.



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DDI2  
HDMI x 4 lanes

eDP



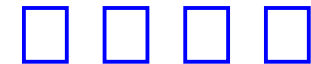
page 28

eDP

DDI

Interleaved Memory

DDR4-ON BOARD 4G 8Gb x16



page 19

260pin DDR4-SO-DIMM X1



page 20

Memory BUS  
Dual Channel

1.2V DDR4 2400

USB 3.0  
conn x1  
USB3 port 1  
USB2 port 1

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USB 2.0  
conn x2  
USB2 port2 (MB)  
USB2 port4(SUB)

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CMOS  
Camera  
USB2 port 7

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Card Reader  
RTS5140  
Reserved

USB2 port 6(SUB)

Finger  
Printer  
USB2 port 5Nvidia N17S-G0/G2  
with GDDR5 x2

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PCIe 3.0 x 4  
8GT/s  
port 1-4SATA Gen 3  
6.0 Gb/s  
(SATA2)PCIe 3.0 x4  
8GT/s  
Port 9-12Flexible IO  
Base-U PCIe 3.0x2 (CML)PCIe 1.0  
2.5GT/s  
port 6PCIe 1.0  
2.5GT/s  
port 5SATA Gen 3  
6.0 Gb/s  
port 0  
(SATA0)SATA Gen 1  
1.5 Gb/s  
port 1  
(SATA1A)LAN(GbE)  
Realtek 8111H  
page 30

RJ45 conn.

SATA HDD  
Conn.

page 33

SATA ODD  
Conn.Intel Whiskey lake U  
Intel Comet lake U

Processor

Cannon Lake PCH-LP

46x24 mm

15W

1528pin BGA  
page 07~18WHL-U 4+2  
WHL-U 2+2

LPC/eSPI BUS

CLK=24MHz

ENE  
KB9022

page 36

Int.KBD



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Touch Pad  
PS2 (from EC) / I2C (from SOC)  
USB2 port 8 (FP)

page 37

USBx8 48MHz

HD Audio

3.3V 24MHz

SPI

SPI ROM  
128Mb page 9HDA Codec  
ALC255  
page 32Touch  
ScreenUSB2 port 3  
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Int. Speaker



page 32

Int. DMIC  
on Camera

page 28

UAI

page 35

Sub Board

LS-H802P  
HDD/B  
page 33LS-H783P  
LID/B  
page 38LS-H781P  
IO/B  
page 38LS-H784P  
ODD/B  
page 33Fan Control  
page 39RTC CKT.  
page 15Power On/Off CKT.  
page 37DC/DC Interface CKT.  
page 40Power Circuit DC/DC  
page 41~54

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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<b>Vcc</b>	<b>3.3V +/- 5%</b>					
<b>Ra</b>	<b>100K +/- 1%</b>					
<b>Board ID</b>	<b>Rb</b>	<b>V<sub>BID</sub> min</b>	<b>V<sub>BID</sub> typ</b>	<b>V<sub>BID</sub> max</b>	<b>EC AD3</b>	<b>PCB Revision</b>
<b>0</b>	<b>0</b>	<b>0 V</b>	<b>0 V</b>	<b>0.300 V</b>	<b>0x00 - 0x13</b>	<b>0.1 (EVT)</b>
<b>1</b>	<b>12K +/- 1%</b>	<b>0.347 V</b>	<b>0.345 V</b>	<b>0.360 V</b>	<b>0x14 - 0x1E</b>	<b>0.2 (DVT)</b>
<b>2</b>	<b>15K +/- 1%</b>	<b>0.423 V</b>	<b>0.430 V</b>	<b>0.438 V</b>	<b>0x1F - 0x25</b>	<b>0.3 (PVT)</b>
<b>3</b>	<b>20K +/- 1%</b>	<b>0.541 V</b>	<b>0.550 V</b>	<b>0.559 V</b>	<b>0x26 - 0x30</b>	<b>1.0 (PreMP)</b>
<b>4</b>	<b>27K +/- 1%</b>	<b>0.691 V</b>	<b>0.702 V</b>	<b>0.713 V</b>	<b>0x31 - 0x3A</b>	
<b>5</b>	<b>33K +/- 1%</b>	<b>0.807 V</b>	<b>0.819 V</b>	<b>0.831 V</b>	<b>0x3B - 0x45</b>	
<b>6</b>	<b>43K +/- 1%</b>	<b>0.978 V</b>	<b>0.992 V</b>	<b>1.006 V</b>	<b>0x46 - 0x54</b>	
<b>7</b>	<b>56K +/- 1%</b>	<b>1.169 V</b>	<b>1.185 V</b>	<b>1.200 V</b>	<b>0x55 - 0x64</b>	

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CODEC	255@/256@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
CNVi /BT PCM Select	CNVI@/PCM@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
TPM	TPM@
Finger Print	FP@/FPFMC@
Finger print power	FP3V@/FP5V@
UMA or DGPU	UMA@/VGA@
CPU Select	WHL@/CML@
SATA/ODD select	RD@/NRD@/ODD@
USB charger	CHG@

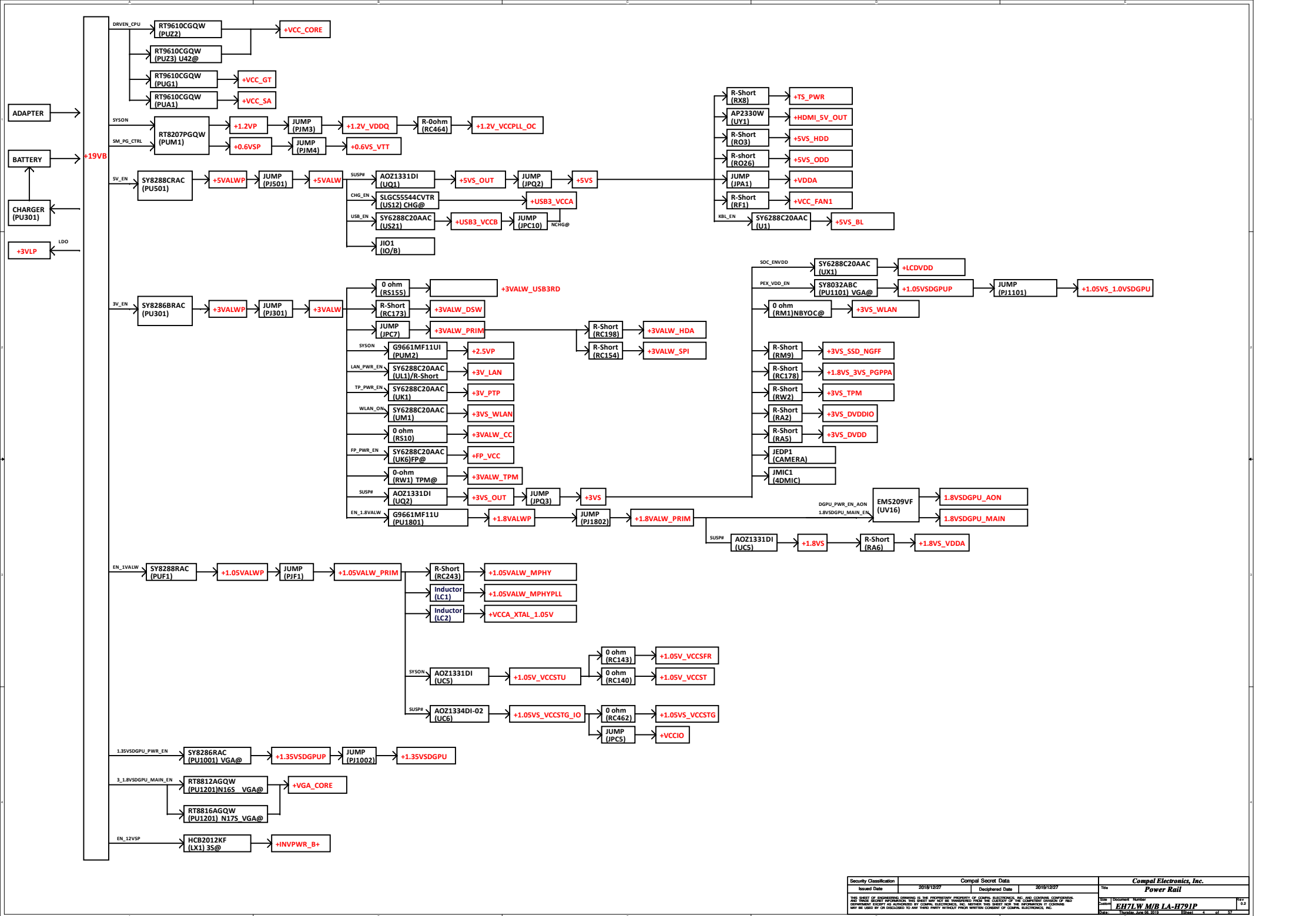
BOM Option Table	
Item	BOM Structure
MB Stage	EVT@/DVT@/PVT@/MP@
G Sensor	GSEN@
For over 3 cell battery	3S@
MD BOM Select	NOX76@/X76DSAM@/ X76DMIC@/X76DHYN@/
VRAM BOM Select	X76VSAM@/X76VMIC@/ X76VHYN@/
Memory related	SPD@/DDP@/MEM@
CPU C10 support	C10@
BOM select	15DIS@/15@/
VGA chip	G0@/G2@

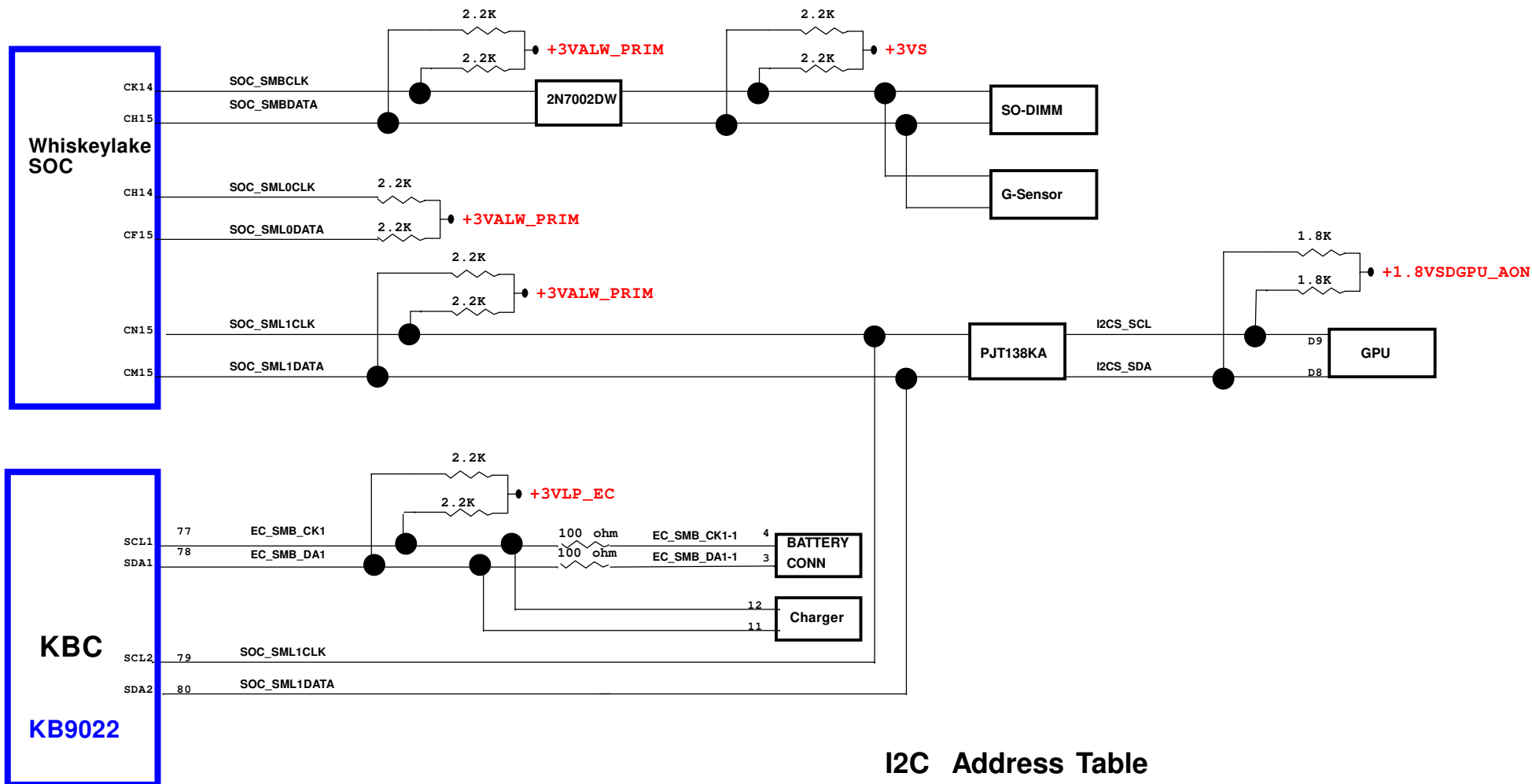
43 Level	Description	BOM Structure
431AHVBOL01	SMT MB AH791 EH7LW I37020U22 230 HDMI	814508/PCB8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VHYNE/NC108/CNV18/NCHG8/FP8/3S8/LPC8/CMC8/GSENE/RD8/ODD8/2558/BYOC8/TPM8/EVT8/X4E8/158/15D1S8/FP3V8
431AHVBOL02	SMT MB AH791 EH7LW I38130U42 250 HDMI	826508/PCB8/MEM8/SDP8/X76DHYNE/VGA8/G28/X76VHYNE/NC108/CNV18/NCHG8/FP8/3S8/LPC8/CMC8/GSENE/RD8/ODD8/2558/BYOC8/TPM8/EVT8/X4E8/158/15D1S8/FP3V8
431AHVBOL03	SMT MB AH791 EH7LW I38145U22 230 HDMI	814508/PCB8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VHYNE/NC108/CNV18/NCHG8/RD8/ODD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/178/
431AHVBOL04	SMT MB AH791 EH7LW I58265U42 230 HDMI	826508/PCB8/WHL8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VHYNE/NC108/CNV18/NCHG8/RD8/ODD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/178/
431AHVBOL05	SMT MB AH791 EH7LW I38145U22 230V8 HDMI	814508/PCB8/WHL8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VSAME/NC108/CNV18/NCHG8/RD8/ODD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/178/
431AHVBOL06	SMT MB AH791 EH7LW I58265U42 230V8 HDMI	826508/PCB8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VSAME/NC108/CNV18/NCHG8/RD8/ODD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/178/
431AHVBOL51	SMT MB AH791 EH5LW I38145U22 230 HDMI	814508/PCB8/WHL8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VHYNE/NC108/CNV18/NCHG8/NRD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/158/15D1S8/
431AHVBOL52	SMT MB AH791 EH5LW I58265U42 230 HDMI	826508/PCB8/WHL8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VHYNE/NC108/CNV18/NCHG8/NRD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/158/15D1S8/
431AHVBOL53	SMT MB AH791 EH5LW I38145U22 230V8 HDMI	814508/PCB8/WHL8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VSAME/NC108/CNV18/NCHG8/NRD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/158/15D1S8/
431AHVBOL54	SMT MB AH791 EH5LW I58265U42 230V8 HDMI	826508/PCB8/MEM8/SDP8/X76DHYNE/VGA8/G08/X76VSAME/NC108/CNV18/NCHG8/NRD8/3S8/LPC8/CMC8/2558/DVT8/X4E8/158/15D1S8/

SIGNAL STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.05VALW_PRIM	+1.05V Always power rail	ON	ON	ON*1
+1.05V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.05VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VSDGPU	+1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON*2	OFF	OFF

Note : ON\*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.  
ON\*2 power plane is ON when DGPU turn on

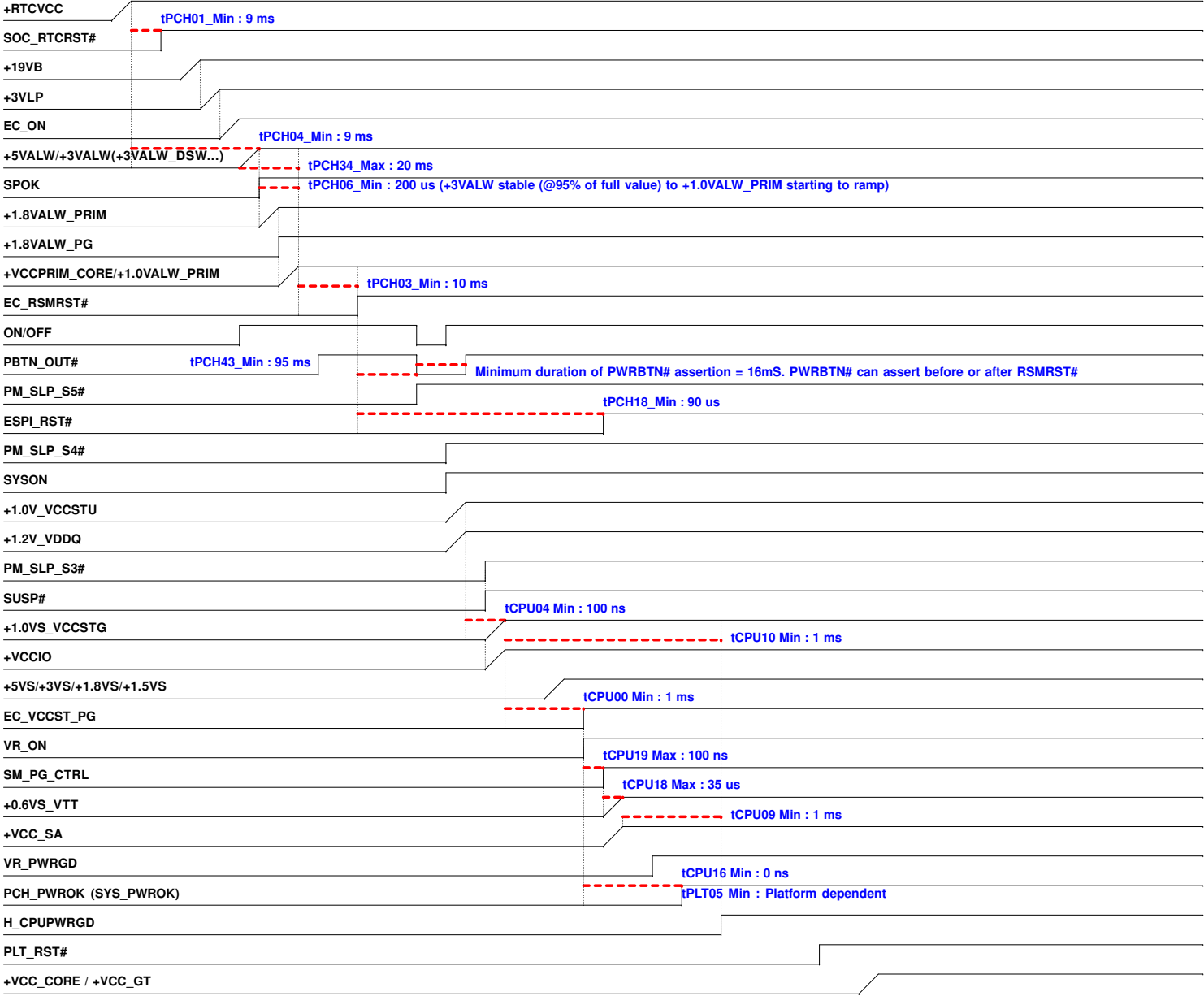




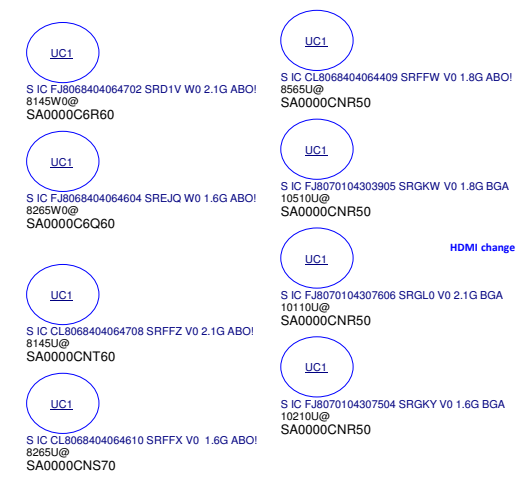
I2C Address Table

BUS	Device	Address (8 bit)
I2C_0 (+3VS)	Reserved	
I2C_1 (+3VALW_PRIM)	TM-P3393-003 (TP)	0x2C
	FA577E-1206 (TP-ELAN)	0x15
	SA577C-12A0 (TP-ELAN)	0x15
SOC_SMBCLK (+3VS)	SO-DIMM2	0xA4
	G-Sensor	0x30
SOC_SML1CLK (+3VALW_PRIM)	GPU	0x9E
	EC	
EC_SMB_CK1 (+3VLP)	BQ24781 (Charger IC)	0x12
	BATTERY PACK	0x16

PWR Sequence\_SKL-U2+2\_DDR3L\_Value\_NON CS



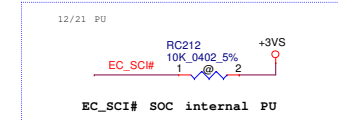
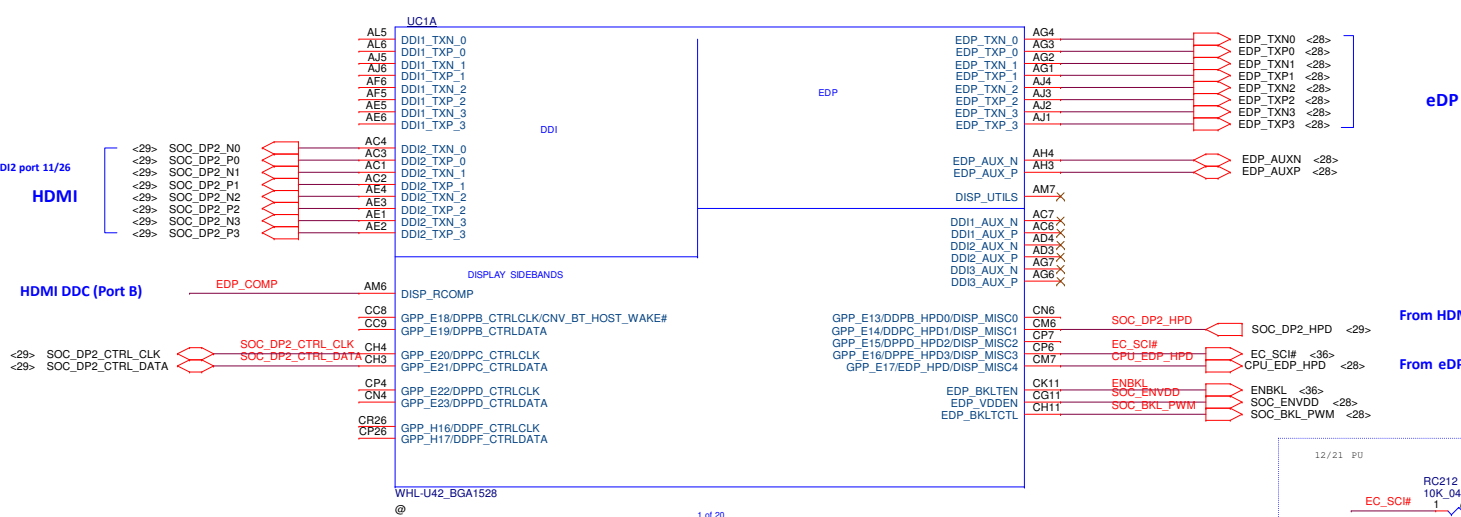
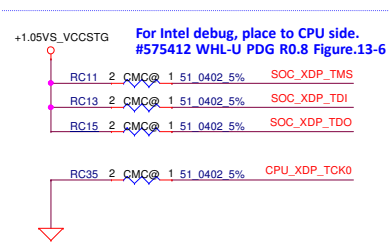
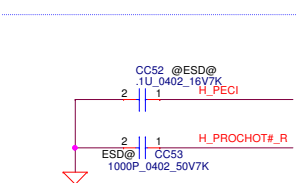
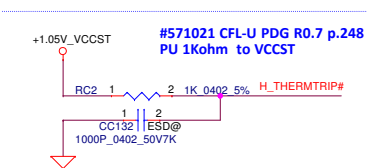
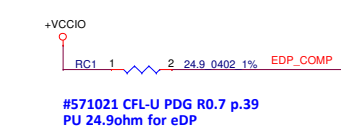
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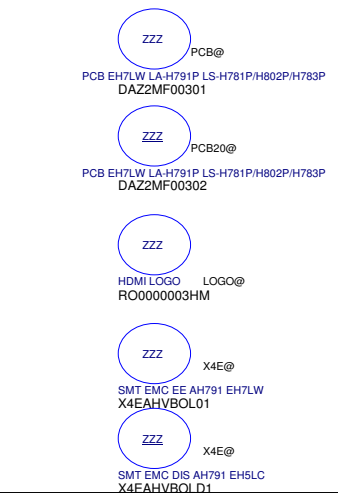
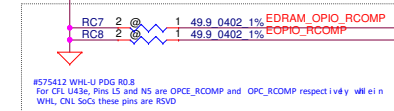
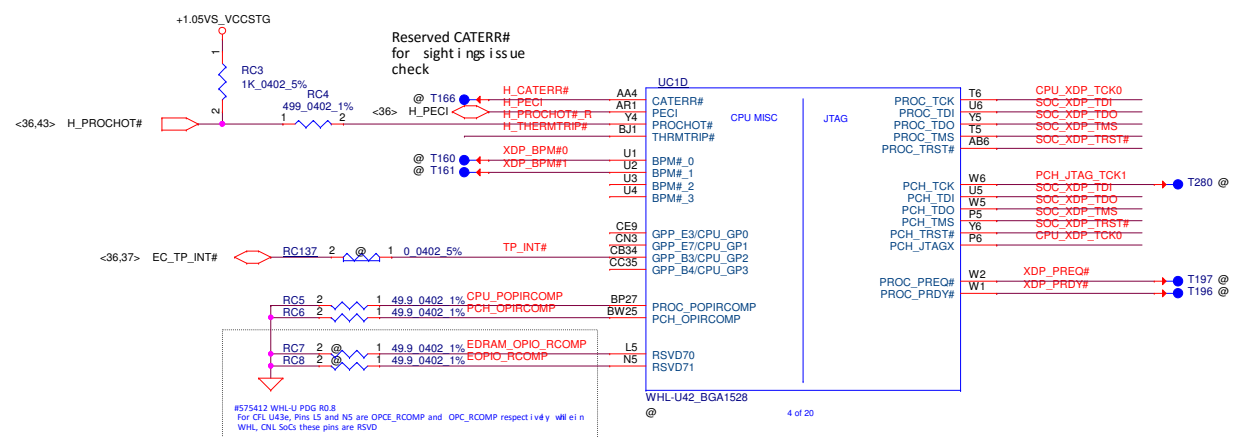
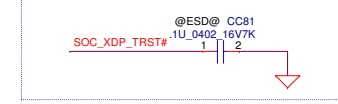
### #571021 CFL-U PDG R0.7 p.104

Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDP0_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	No Connect
Port 2	DDP0_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	
Port 3	DDP0_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	
Port 4	DDP0_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	



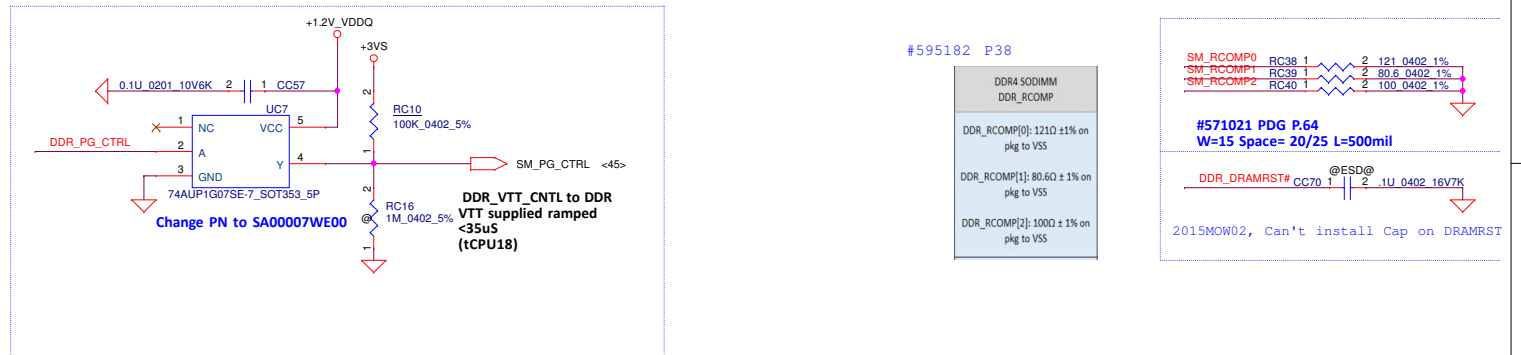
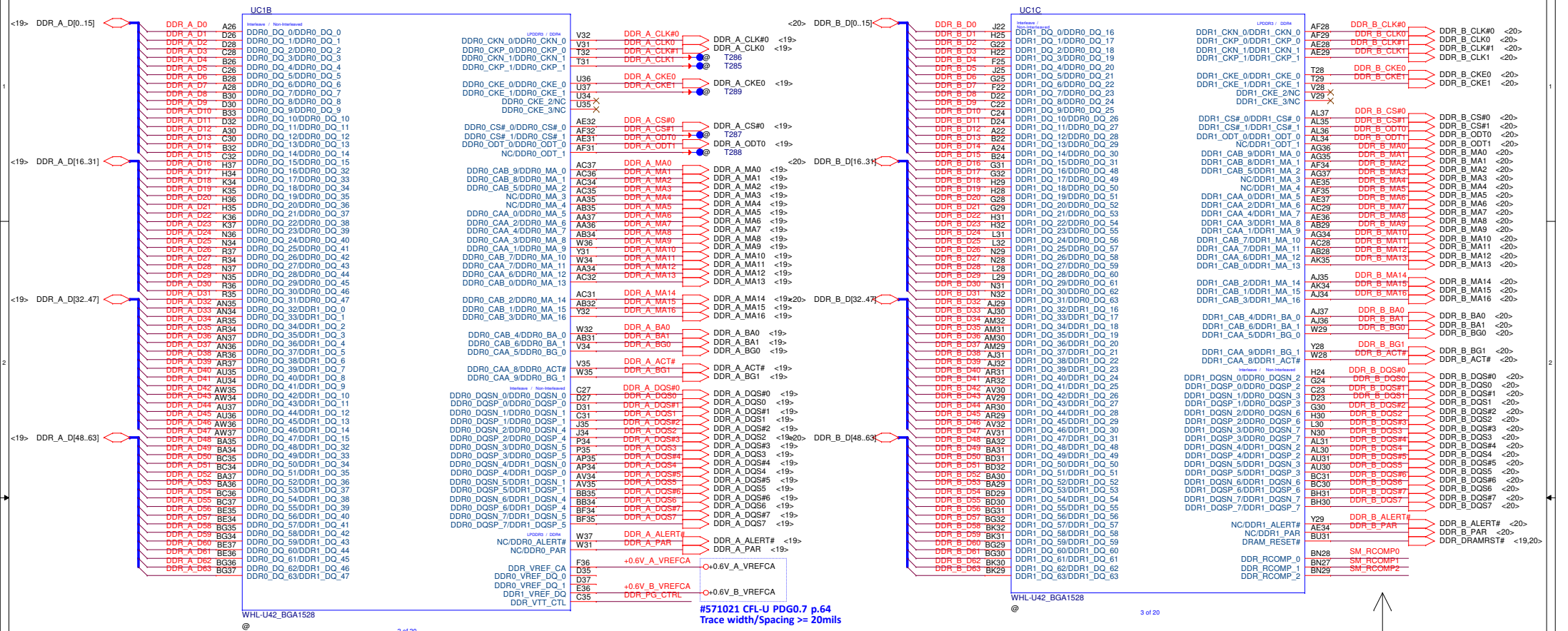
#545659 PCH EDS1.51 P.131  
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.  
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:  
• GPP\_B14 GPP\_B20 GPP\_B23  
• GPP\_C[23 : 22]  
• GPP\_D[4 : 0]  
• GPP\_E[8 : 0], GPP\_E[16 : 13]



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Compal Electronics, Inc.				
WHL-U(1/12)DDI,MSIC,XDP,EDP				
EH7LW M/B LA-H791P				
Date: Friday, August 02, 2019				
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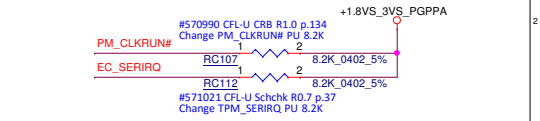
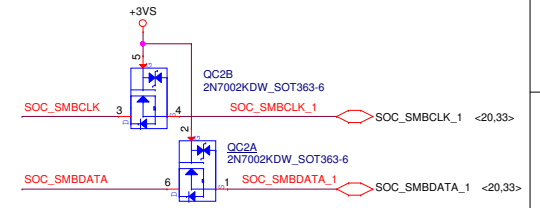
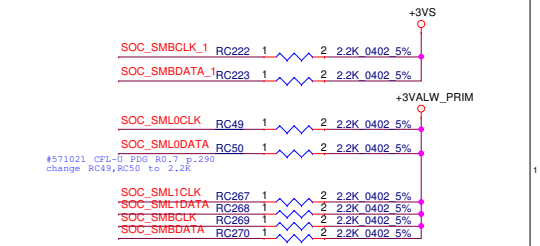
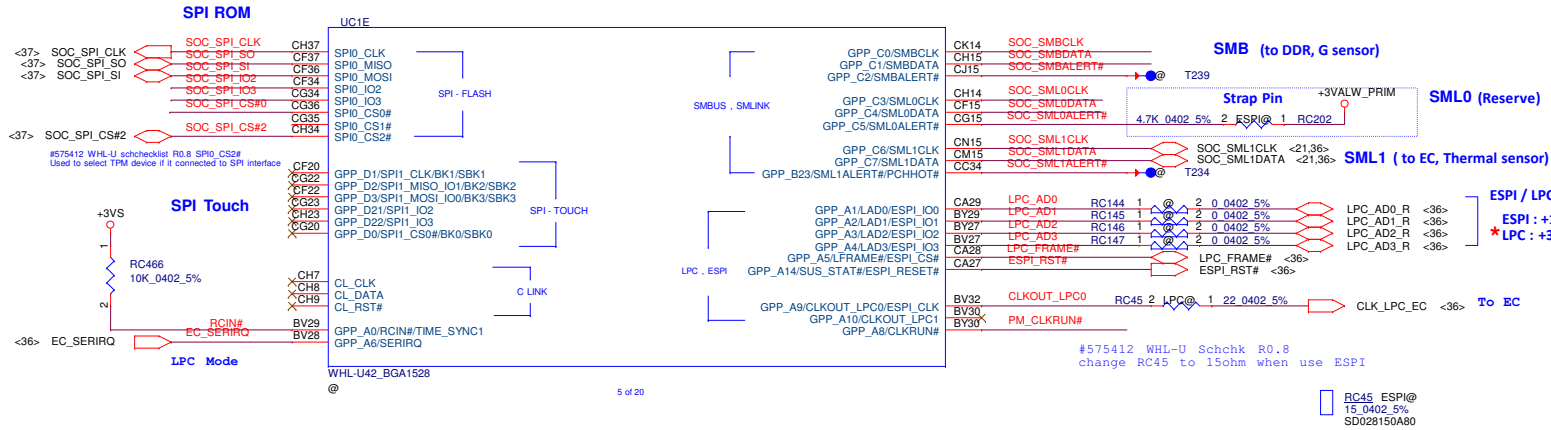


# Interleaved Memory



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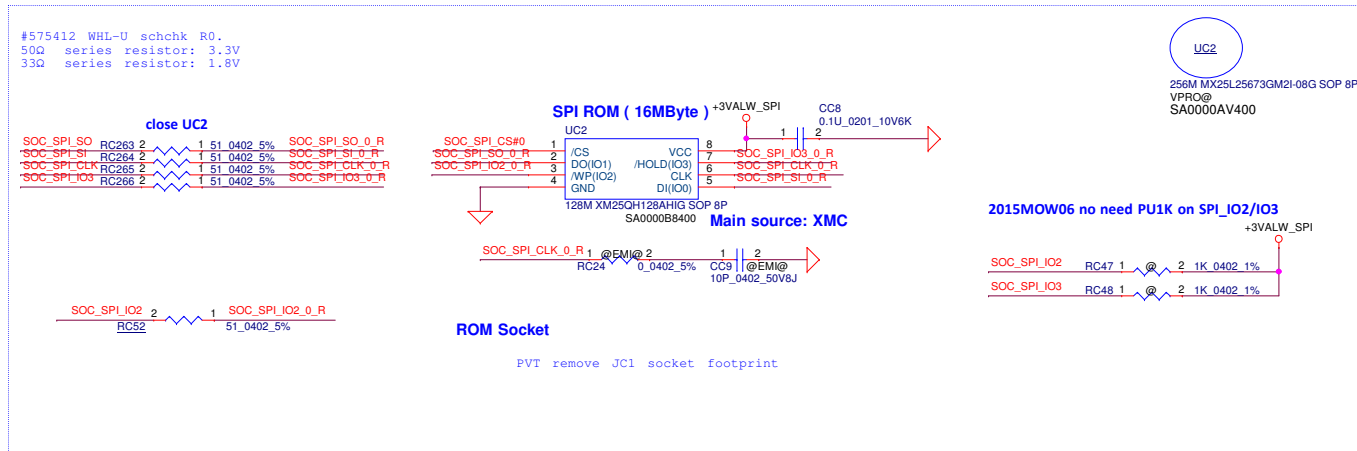


**SML0ALERT# / GPP\_C5 (Internal Pull Down):**  
(Sampled: Rising edge of RSMRST# )

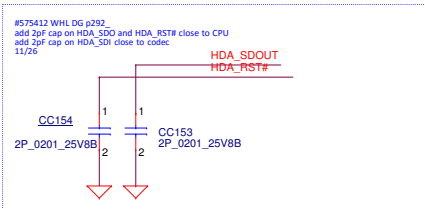
**eSPI or LPC**  
\* 0 = LPC is selected for EC --> For KB9022/9032 Use  
1 = eSPI is selected for EC --> For KB9032 Only.

**SMBALERT# / GPP\_C2 (Internal Pull Down):**  
(Sampled: Rising edge of RSMRST# )

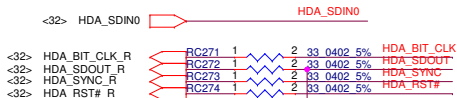
**TLS Confidentiality**  
\* 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)  
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



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## HDA for AUDIO



### HDA\_SDO / I2S\_TXD0 (Internal Pull Down):

(Sampled: Rising edge of PCH\_PWROK)

Flash Descriptor Security Override

0 = Enable security measures defined in the Flash Descriptor.

1 = Disable Flash Descriptor Security (override). This

strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

### SPKR / GPP\_B14 (Internal Pull Down):

(Sampled: Rising edge of PCH\_PWROK)

### TOP Swap Override

0 = Disable TOP Swap mode.

1 = Enable TOP Swap Mode.

### Intel HD Audio link capabilities

> Two SDI signals to support two external codecs.

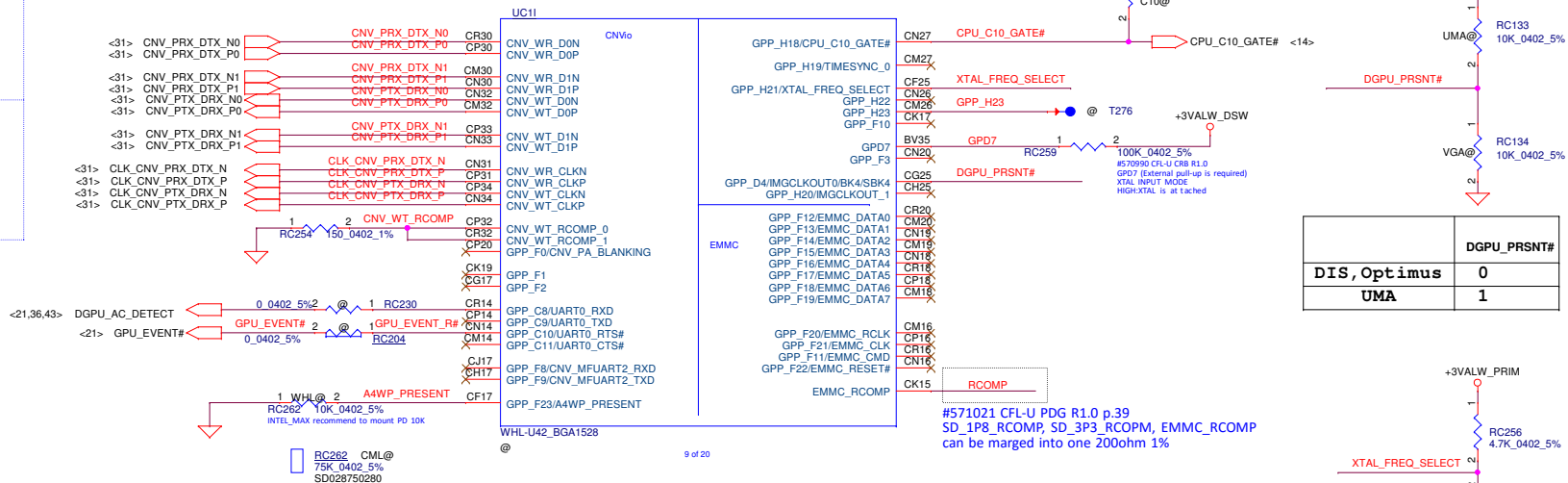
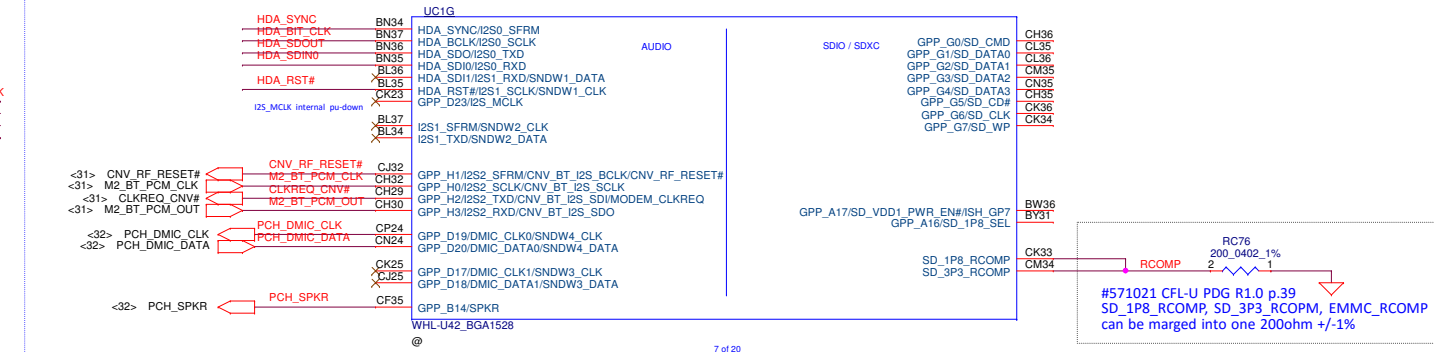
> Drivers variable frequency (5MHz to 24MHz) BCLK to support:

-- SDO double pumped up to 48 Mb/s

-- SDI's single pumped up to 24 Mb/s

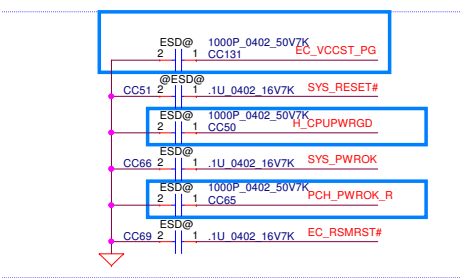
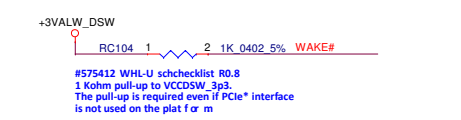
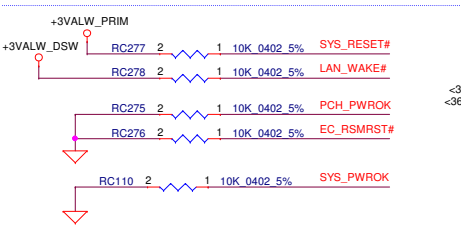
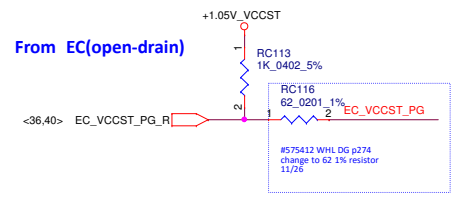
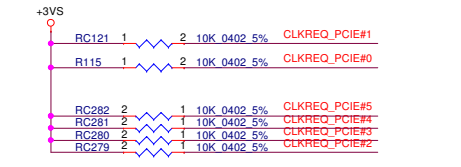
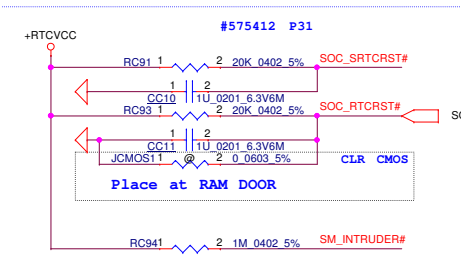
> Provides cadence for 44.1 kHz based sample rate output.

> Support 1.5V, 1.8V, and 3.3V modes.



	DGPU_PRSN#
DIS,Optimus	0
UMA	1

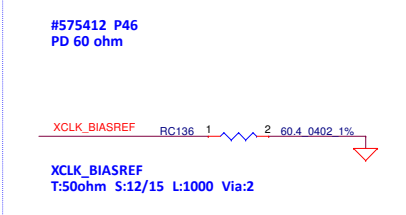
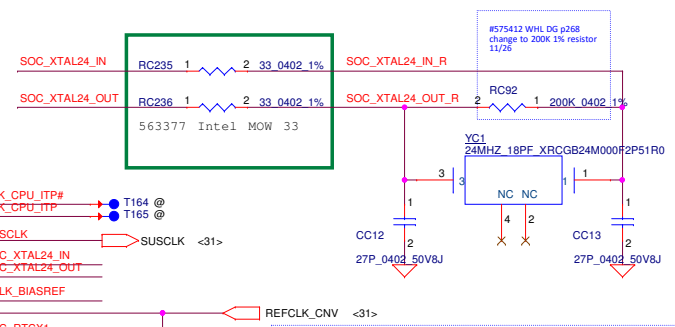
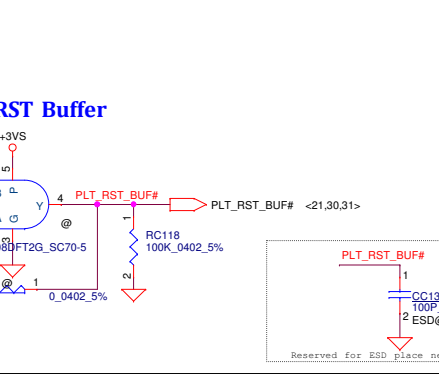
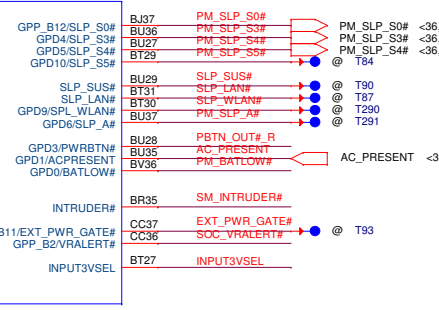
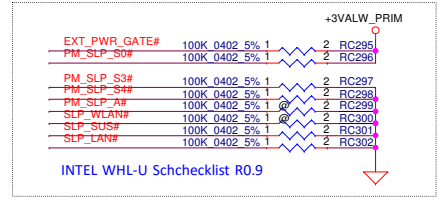
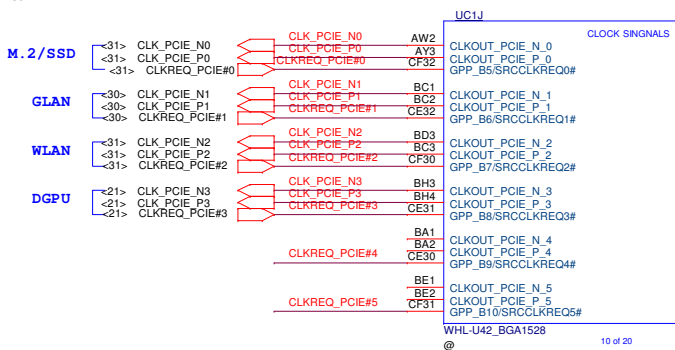
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Issued Date				2018/12/27				Title			
Deciphered Date				2019/12/27				WHL-U(4/12)HDA,EMMC,SDIO,CNV			
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Date				Thursday, June 06, 2019				Sheet 10 of 57			



**#543016 PDG2.0 P.599**

PROCPRWDG is used only for power sequence debug and is not required to be connected to anything on the plat f or m

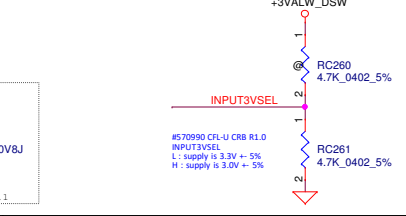
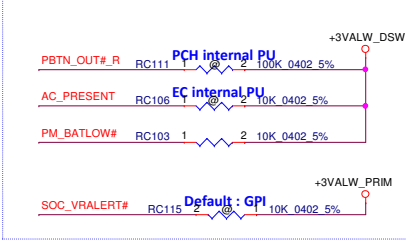
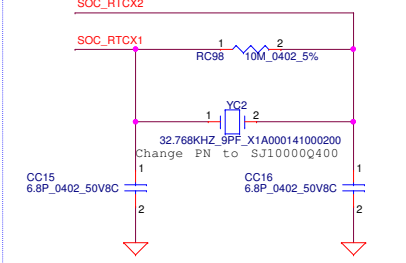
For layout routing ,PCIE CLK P0/P3 exchange



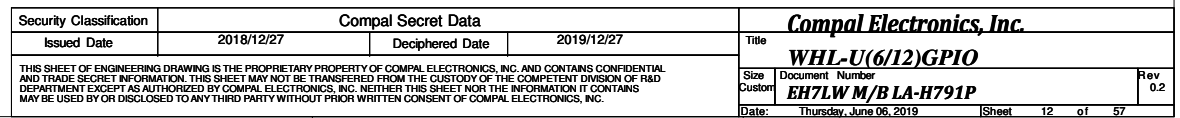
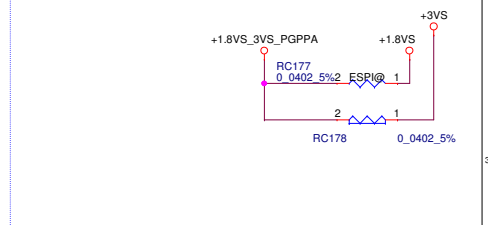
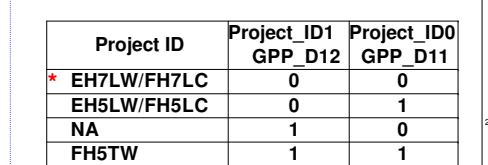
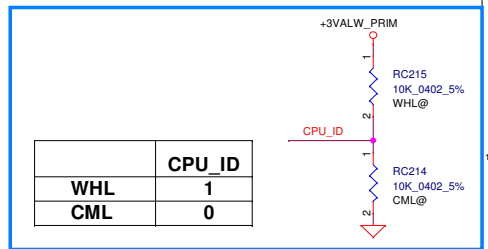
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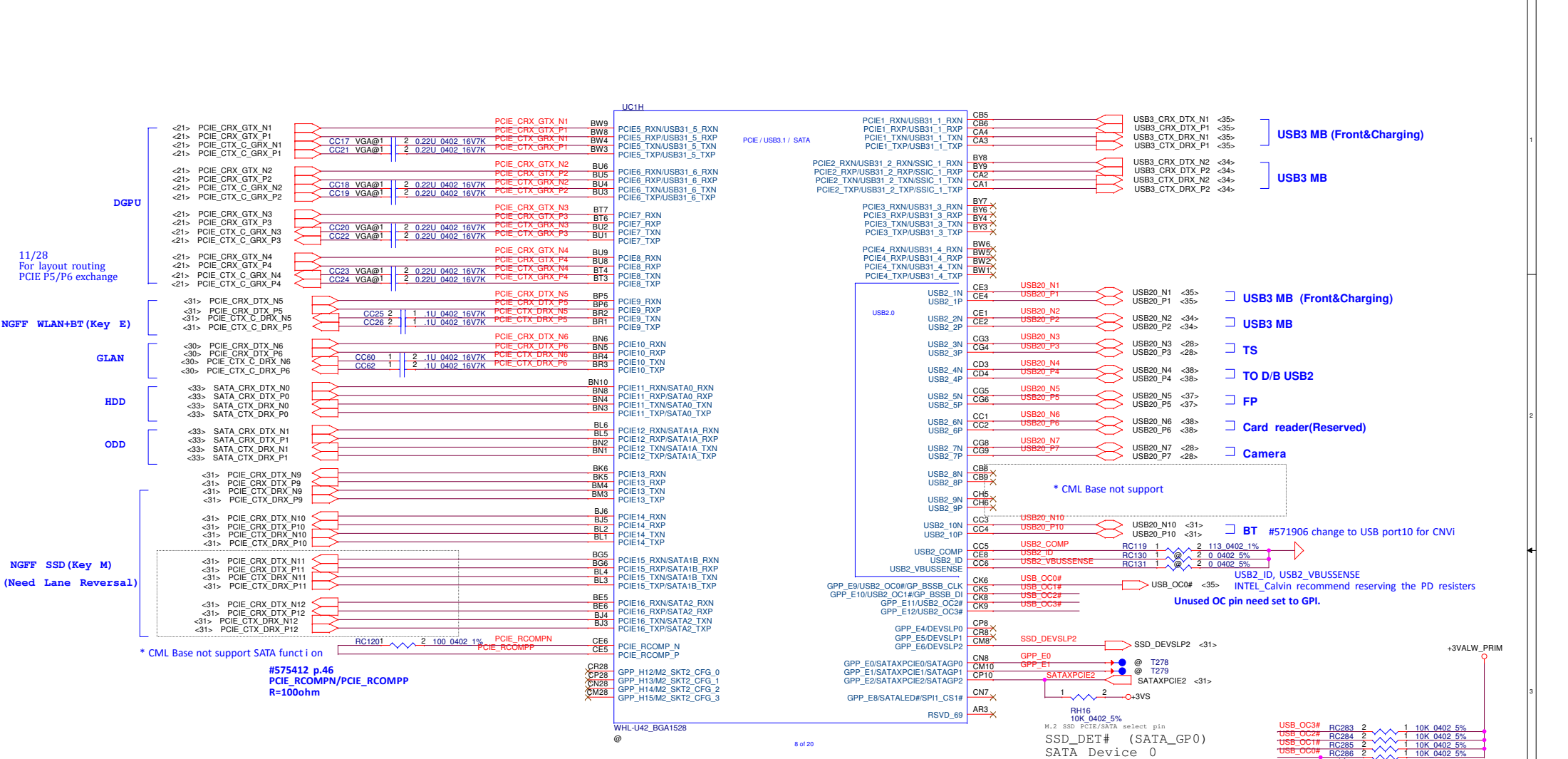
Skylake-U use 24M 50 ohm ESR

Cannonlake U use 38.4M 30 ohm ESR



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				WHL-U(5/12)CLK,GPIO		EH7LW M/B LA-H791P		0.2	
				Date: Thursday, June 06, 2019		Sheet 11 of 57			





6.1.2.1 Cannon Lake U (CNL U) PCH-LP

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

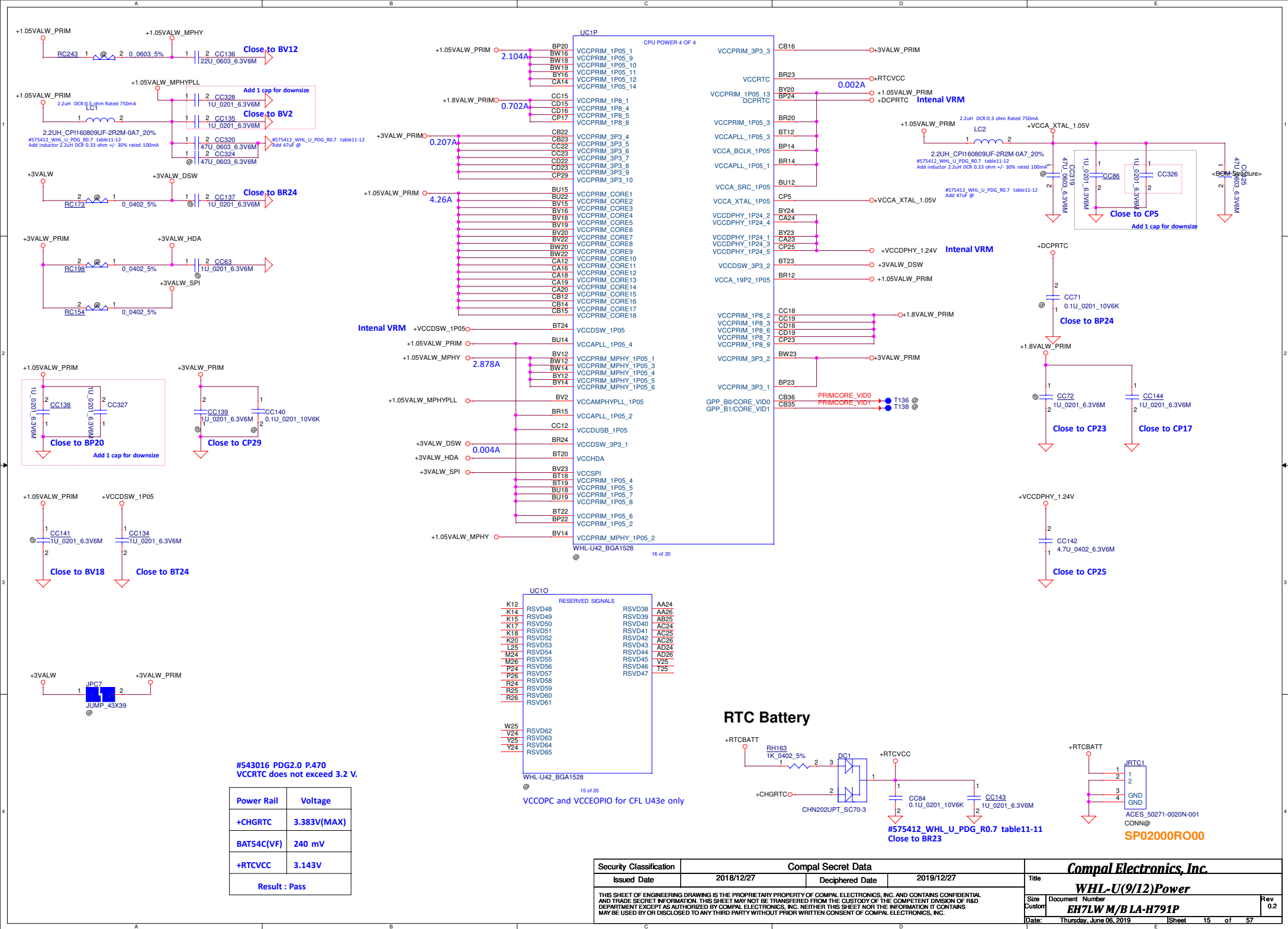
GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

**DEVSLP[2:0] Implementation**  
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.  
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.  
• When high DEVSLP requests the SATA device to enter into the DEVSLP power state  
• When low DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

**SATA General Purpose (SATAGP[2:0]) Signals**  
• The processor provides three SATA general purpose input signals SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.  
• When used as anti-lock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.  
If mechanical presence switches will not be used on the platform SATAGP[2:0] signals can be configured as GPP\_E[2:0] GPIOs signals.



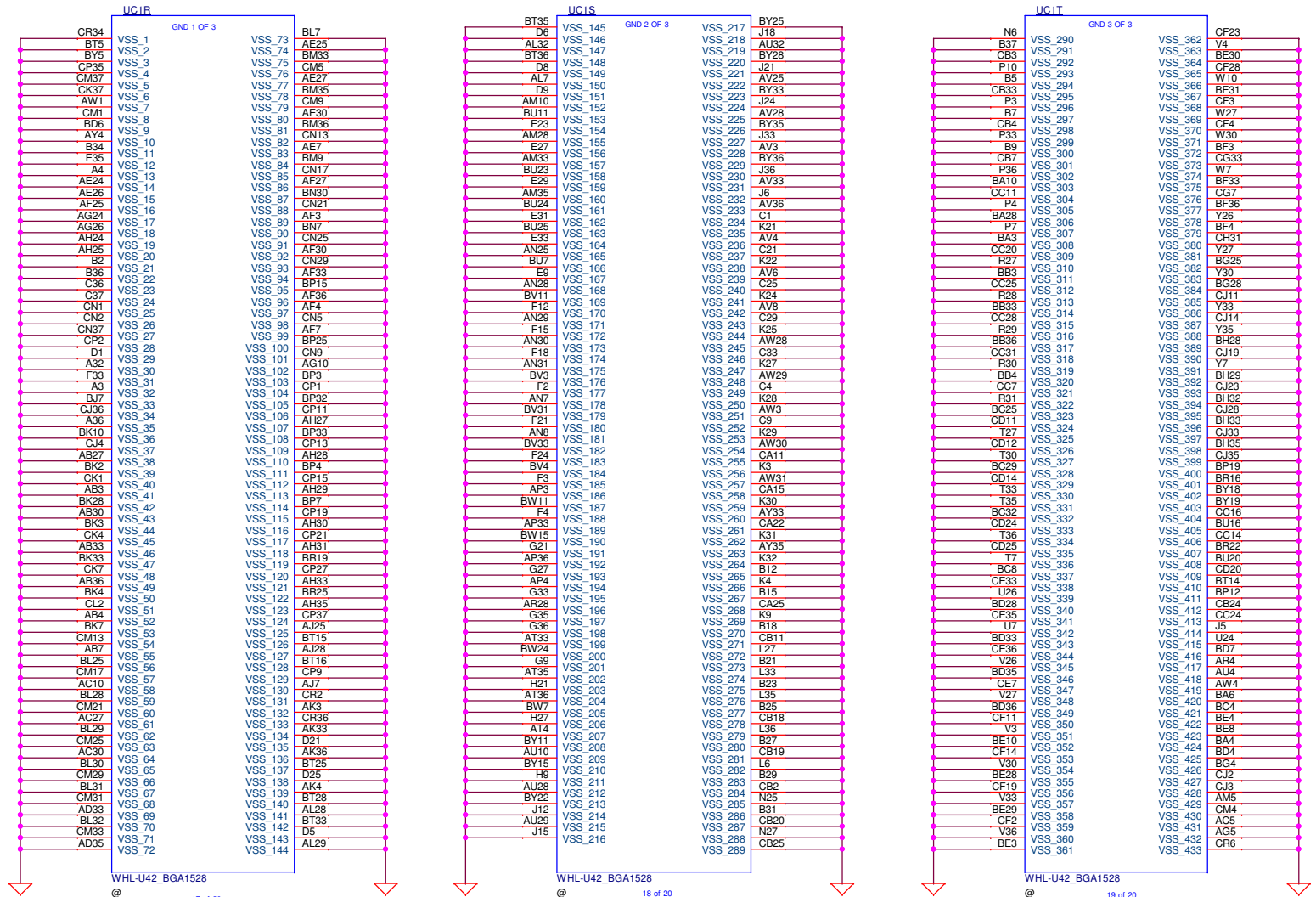




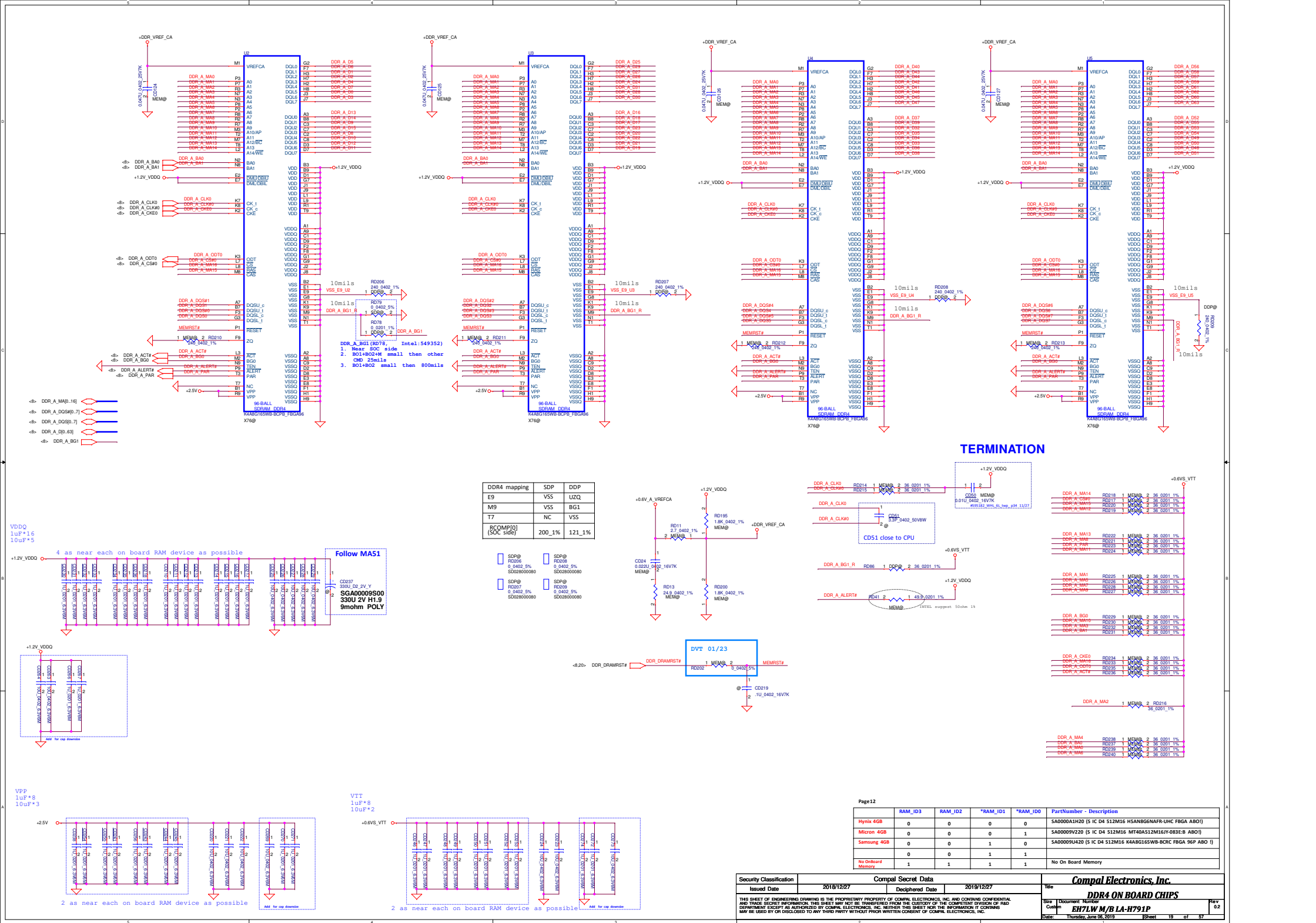


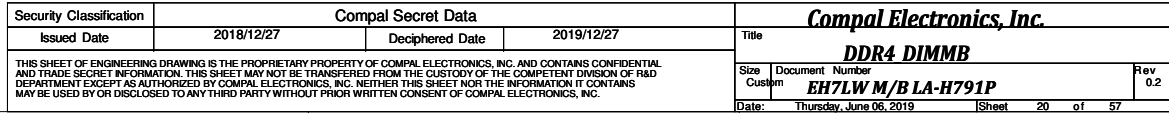


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
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				Custom	<b>EH7LW M/B LA-H791P</b>	0.2
				Date:	Thursday, June 06, 2019	Sheet 16 of 57

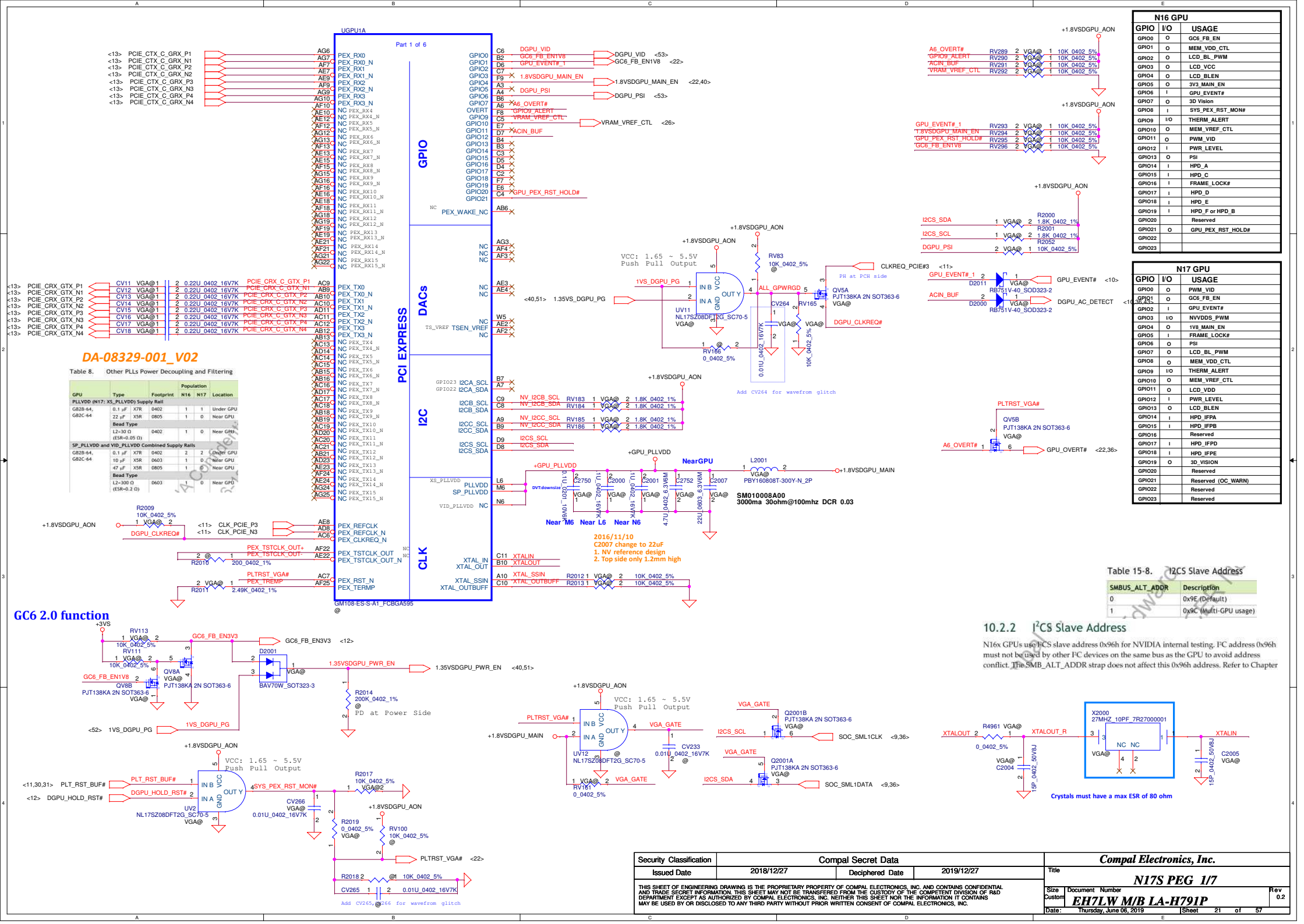




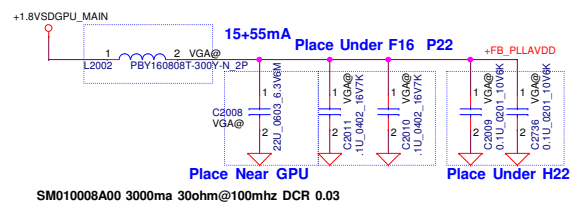
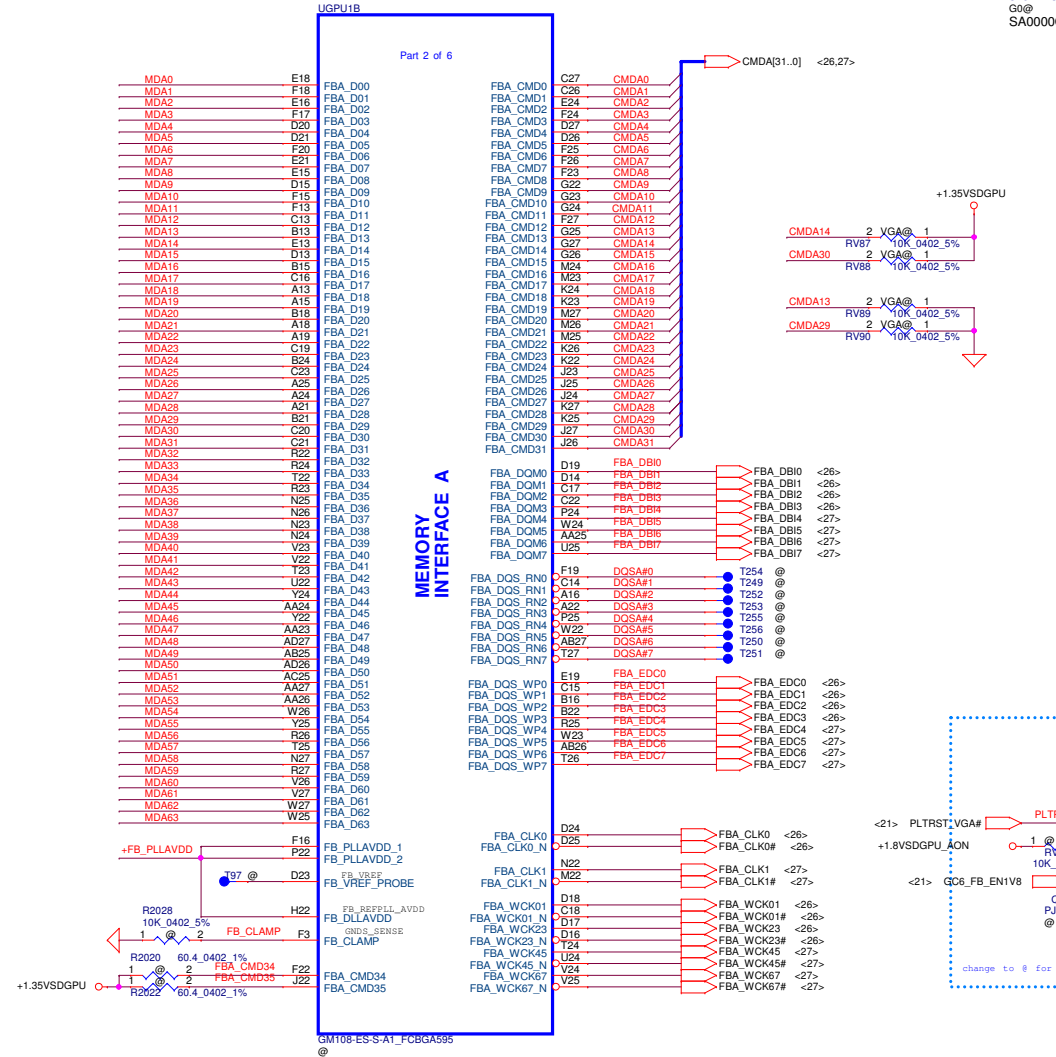
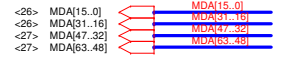






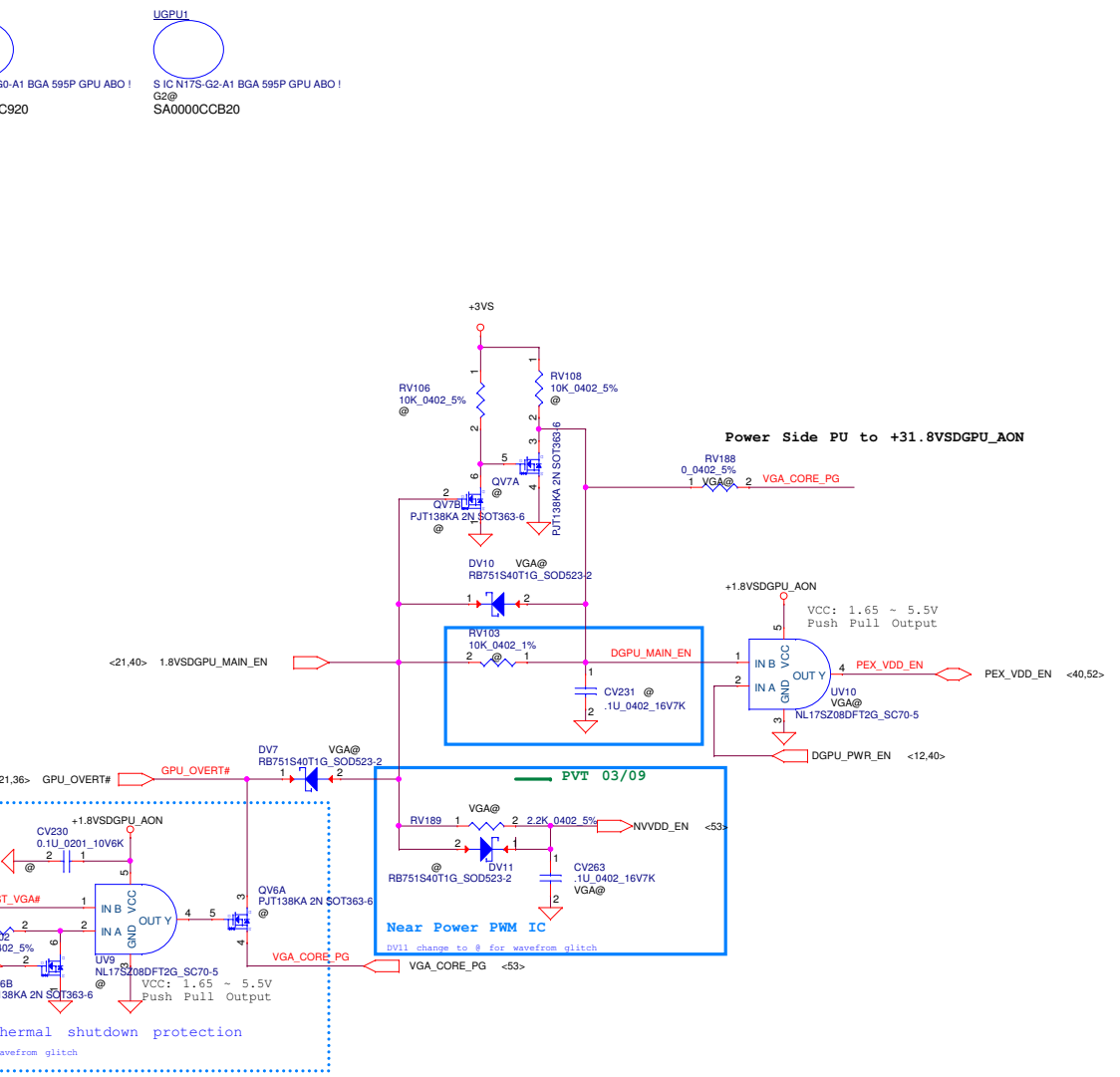


VRAM Interface



DA-08329-001 V01  
Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	4	Under GPU
	22 µF X6S	0805	1	1	Near GPU
Bead Type					
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU



NV 15x DG-06803-V03  
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2
		22 µF	X5R	0805	1
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	1





# NV 16x DG-07158-V05

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1 μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

# DA-08329-001\_V02

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

# NV 16x DG-07158-V05

Table 3-16. PEX\_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

# NV 16x DG-07158-V05

Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR5/BGA-170	1.35V or 1.50V	40.2Ω	40.2Ω	60.4Ω

# NV 16x DG-07158-V05

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU

# DA-08329-001\_V01

Table 9. VDD AON and VDD\_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
N16 3V3_MAIN (N17 VDD18) Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	2
	1.0 µF	X6S	0603	1	1
	4.7 µF	X6S	0603	1	1
N16 3V3_AON (N17 VDD_AON) Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1
	1.0 µF	X6S	0603	1	1
	4.7 µF	X6S	0603	1	1

# NV 16x DG-07158-V05

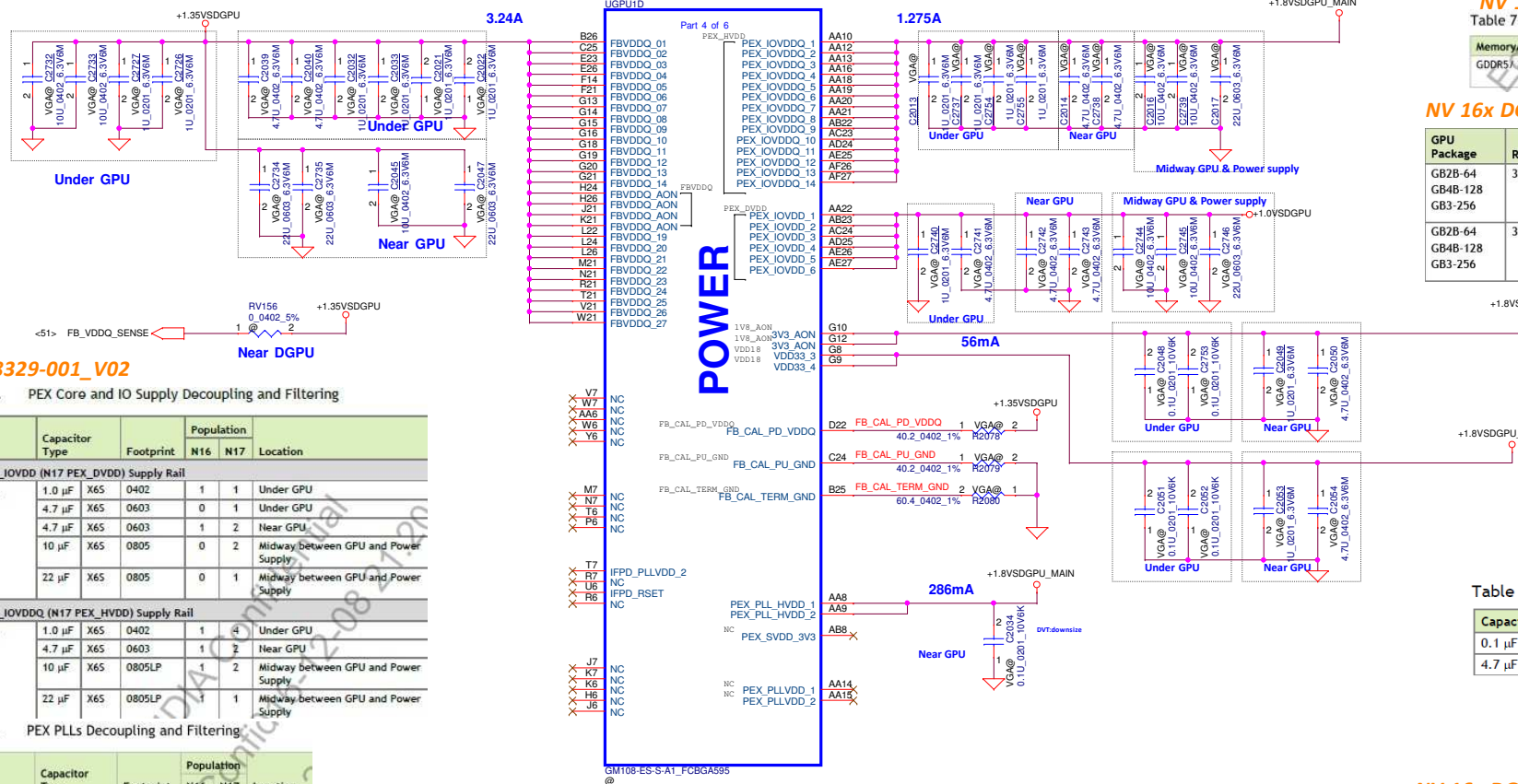
Table 3-18. PEX\_SVDD\_3V3 and PEX\_PLL\_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μF	X7R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

# NV 16x DG-07158-V05

Table 3-17. PEX\_PLLVDD Decoupling

Capacitor Type	Footprint	Population	Location	
0.1 $\mu$ F	X7R	0402	1	Under GPU
1.0 $\mu$ F	X5R	0603	1	Near GPU
4.7 $\mu$ F	X5R	0805	1	Near GPU



GM108-ES-S-A1\_FCBGA595

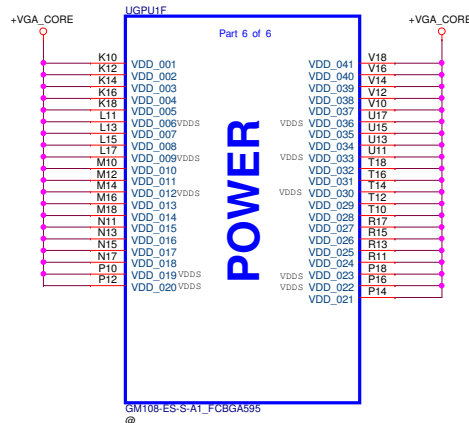
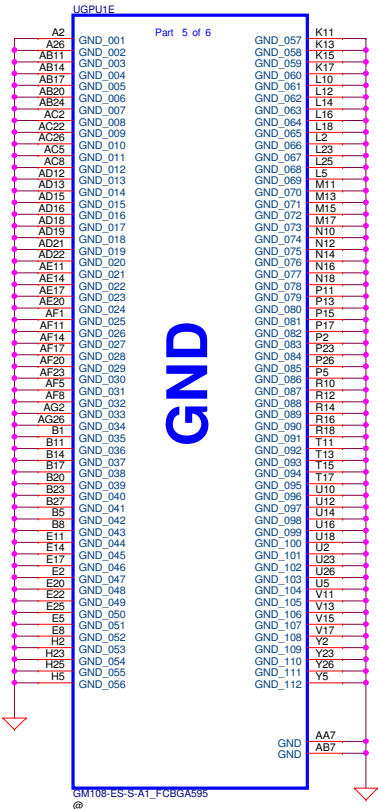
# DA-08329-001\_V02

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
PEX_PLLVDD Supply Rail						
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU



**NV 16x DG-D07158-V05**  
Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64 / GB2C-64	4.7 $\mu$ F X6S	0603	10	10	Under GPU
	1 $\mu$ F X6S	0402	4	4	Under GPU
	47 $\mu$ F X5R	0805	1	1	Near GPU
	22 $\mu$ F X5R	0805	1	1	Near GPU
	4.7 $\mu$ F X5R	0805	5	5	Near GPU
	330 $\mu$ F POS	7343	1	1	Near GPU ESR $\leq$ 6 m $\Omega$

**DA-07750-000-V02**

Table 6. EDP-Continuous<sup>3</sup>

Products	VRAM Type	GPU Core		GPU FBIO		FB Total <sup>1,5</sup>		1.05V Total <sup>2</sup>	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06	0.06
	DDR3/L	21.0	1.4	2.4	2.3	0.80	0.06	0.06	0.06
N165-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06	0.06
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06	0.06
	DDR3/L	26.0	1.4	2.4	2.3	0.80	0.06	0.06	0.06

Table 7. EDP-Peak<sup>3</sup>

Products	VRAM Type	GPU Core		GPU FBIO		FB Total <sup>1,5</sup>		1.05V Total <sup>2</sup>	1.05V Total <sup>2</sup>
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1	2.1	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1	2.1	2.1
N165-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1	2.1	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1	2.1	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1	2.1	2.1

**DA-07751-000-V02**

Table 5. EDP-Continuous<sup>3</sup>

Product	VRAM Type	GPU Core		GPU FBIO		FB Total <sup>1,5</sup>		1.05V Total <sup>2</sup>	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR1	GDDR5 @ 2.0 GHz	18.5	—	2.0	—	4.2	0.8	0.06	0.06
	GDDR5 @ 2.5 GHz	18.5	—	2.0	—	4.7	0.8	0.06	0.06
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8	0.06	0.06

Table 6. EDP-Peak<sup>3</sup>

Products	VRAM Type	GPU Core		GPU FBIO		FB Total <sup>1,5</sup>		1.05V Total <sup>2</sup>	1.05V Total <sup>2</sup>
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR1	GDDR5 @ 2.0 GHz	30.0	—	2.9	—	6.8	2.1	2.1	2.1
	GDDR5 @ 2.5 GHz	31.0	—	3.1	—	7.2	2.1	2.1	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1	2.1	2.1

**SP-08318-001\_V03**

Table 7. Output EDP-Continuous

	NVVDD	GPU FBIO	FB Total <sup>1,5</sup>	1.0V Total <sup>1</sup>	1.8V Total <sup>2</sup>
	—	1.35V <sup>4</sup>	1.35V <sup>4</sup>	1.0V <sup>4</sup>	1.8V <sup>4</sup>
Product	(A)	(A)	(A)	(A)	(A)
N175-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

	NVVDD	GPU FBIO	FB TOTAL <sup>4</sup>	1.0V Total <sup>1</sup>
	—	1.35V <sup>3</sup>	1.35V <sup>3</sup>	1.0V <sup>3</sup>
Product	(A)	(A)	(A)	(A)
N175-G1	60.1	3.2	6.6	0.2

**DA-08329-001\_V01**

Table 3. NVVDD and NVVDS Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
NVVDD Supply Net					
GB2B-64, GB2C-64	4.7 $\mu$ F X6S	0603	10	8	Under GPU
	1 $\mu$ F X6S	0402	4	3	Under GPU
	47 $\mu$ F X5R	0805	1	-	Near GPU
	10 $\mu$ F X7R	0805	-	4	Near GPU
	22 $\mu$ F X5R	0805	1	3	Near GPU
	4.7 $\mu$ F X5R	0805	1	4	Near GPU
	330 $\mu$ F POS	7343	1	1	Near GPU
NVVDS Supply Net					
GB2C-64 Only	4.7 $\mu$ F X6S	0603	N/A	4	Under GPU
	1 $\mu$ F X6S	0402	N/A	2	Under GPU
	10 $\mu$ F X6S	0805	N/A	7	Near GPU
	22 $\mu$ F X6S	0805LP	N/A	1	Near GPU
	330 $\mu$ F POS	7343	N/A	1	Near GPU

VRAM GDDR5 chips GDDR5 Mode H Mapping

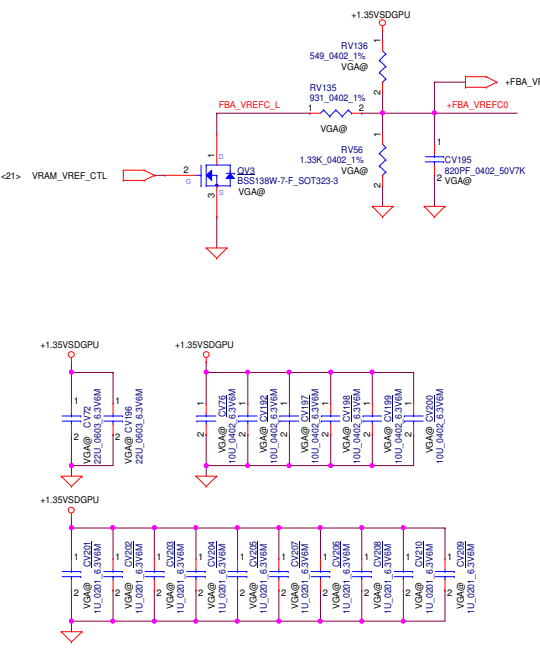
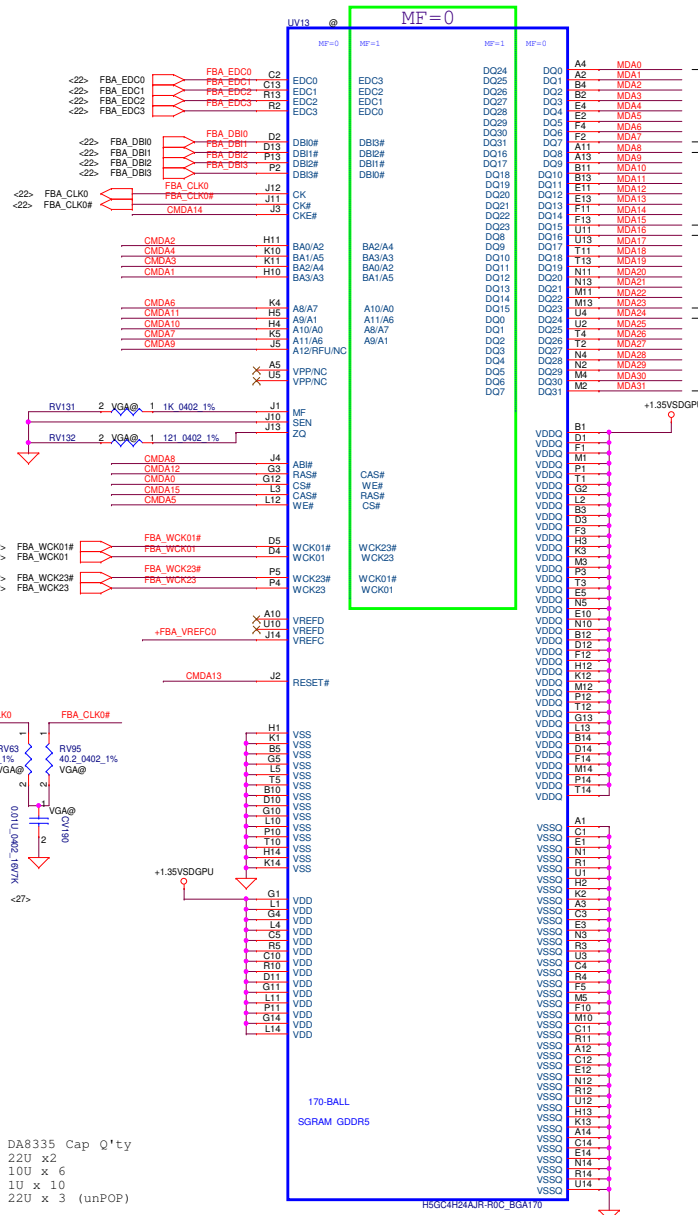


X76 for N17S 2G VRAM

- 777 X76VSAM@
- Samsung\_256Mx32x2 X76829BOL03
- 777 X76VHYN@
- Hynix\_256Mx32x2 X76829BOL01
- 777 X76VMIC@
- Micron\_256Mx32x2 X76829BOL02

	DATA Bus
Address	0...31 32...63
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	AB1#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	AB1#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#

Channel 0 BOT SIDE

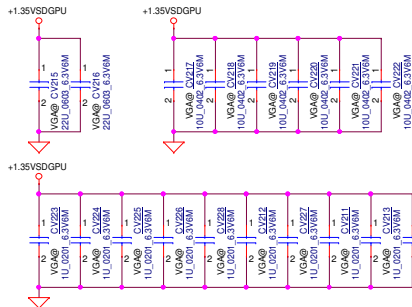
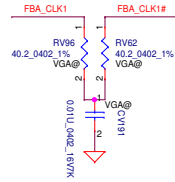


DA8335 Cap Q'ty  
22u x2  
10u x6  
1u x10  
22u x3 (unPOP)

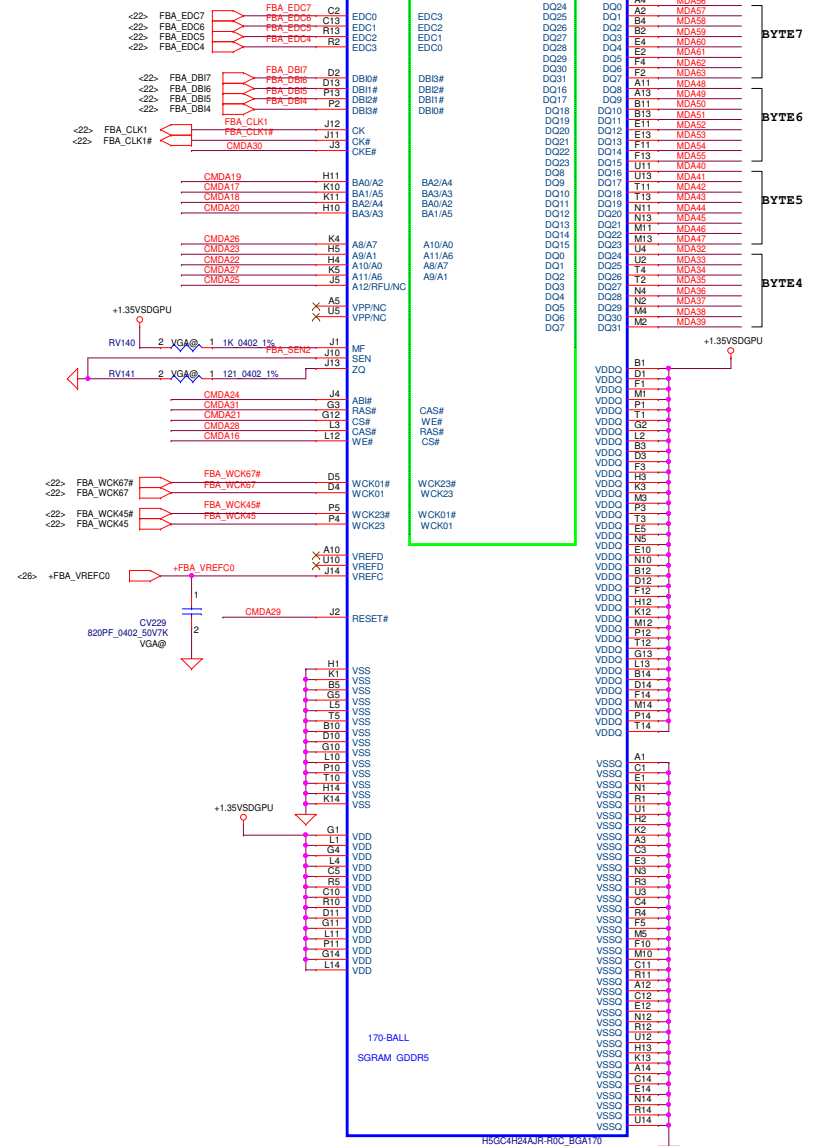


## VRAM GDDR5 chips

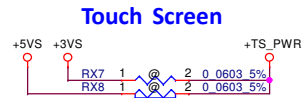
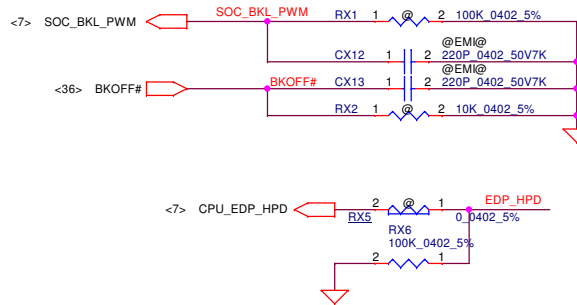
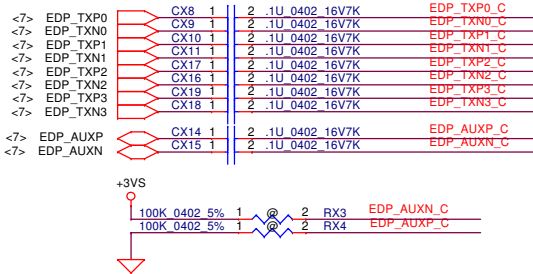
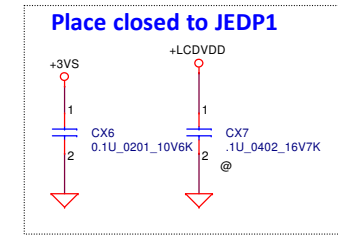
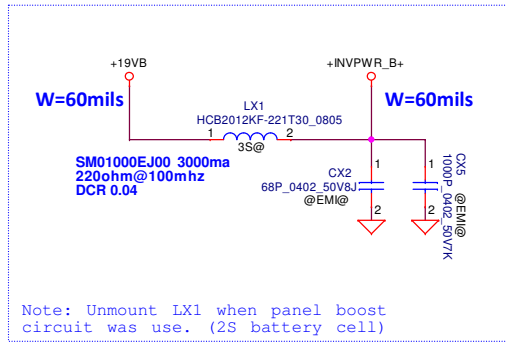
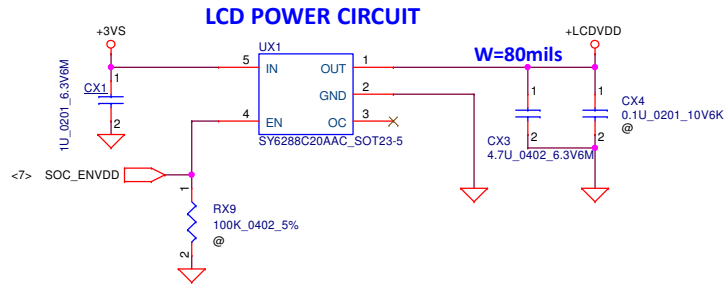
	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#



DA8335 Cap Q'ty  
22U x2  
10U x 6  
1U x 10  
22U x 3 (unPOP)



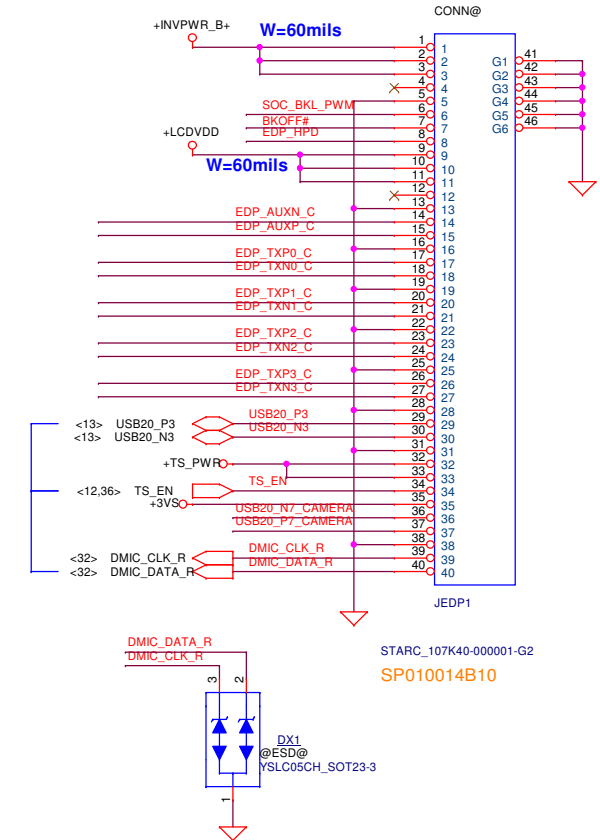
Security Classification	Compal Secret Data			Compal Electronics, Inc.			
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				Custm	EH7LW M/B LA-H791P	0.2	
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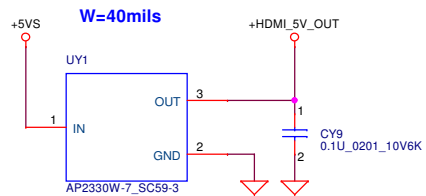
### Camera



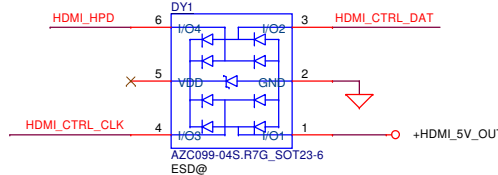
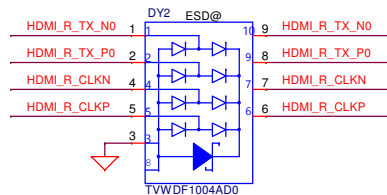
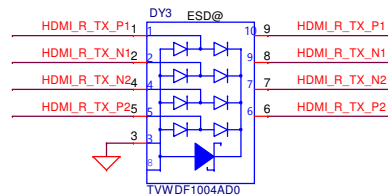
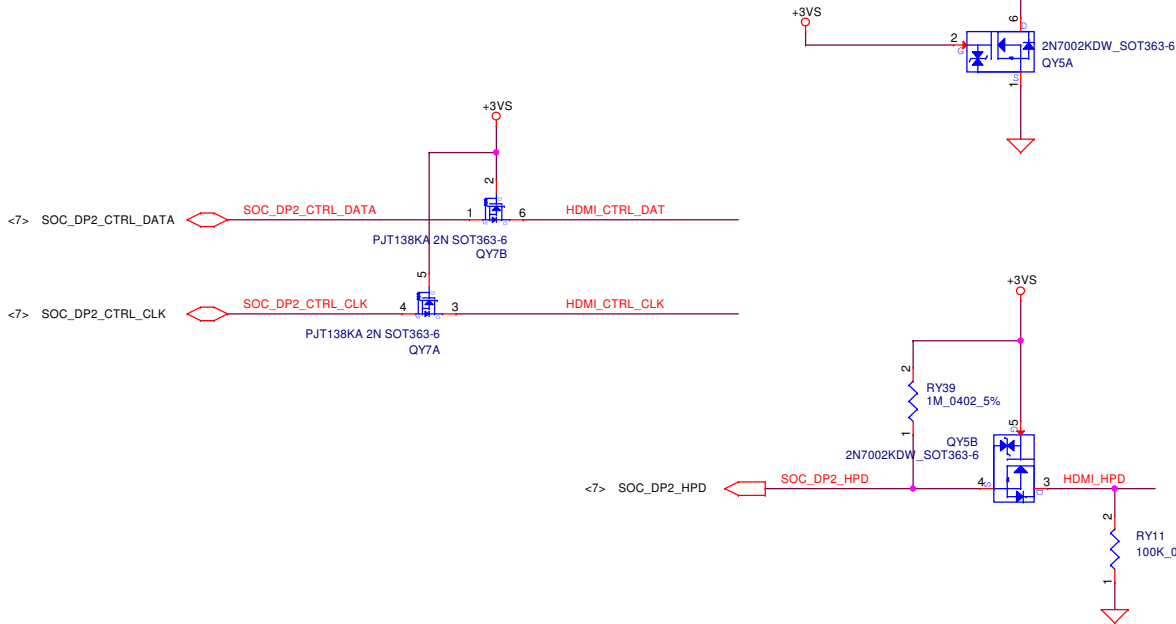
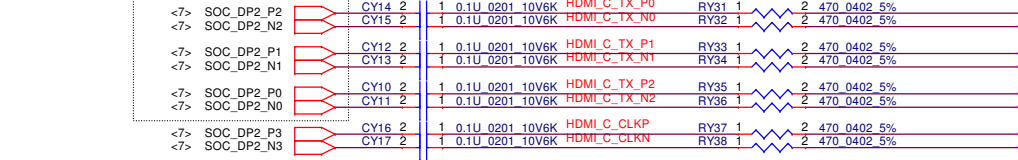
Touch Screen  
For Camera



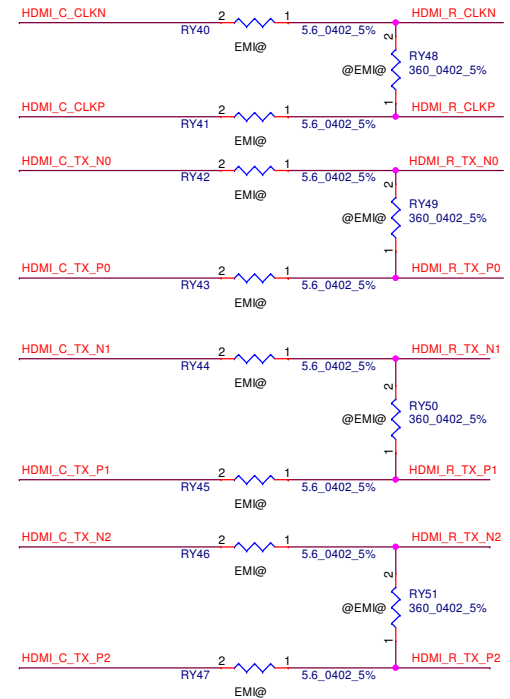
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Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
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Size	Document Number	Rev		0.2	
Custom	EH7LW M/B LA-H791P	Date:		Thursday, June 06, 2019	
Sheet		28		of 57	



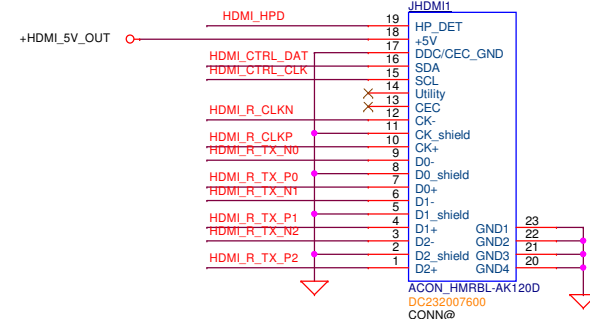
port 0, 2 swap for INTEL HDMI



P/N: SC300001G00,S DIO(BR) AZC099-04S.R7G SOT23 ESD



HDMI connector



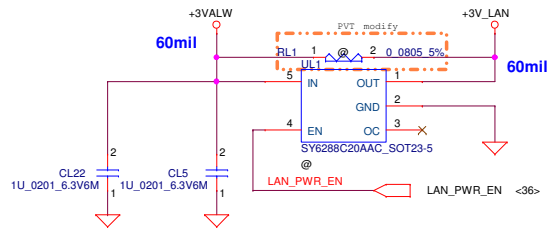
SYMBOL: DC232004700

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2018/12/27		Deciphered Date		2019/12/27		Title	
										HDMI CONN.	
										EH7LW M/B LA-H791P	
										Rev 0.2	
										Date: Thursday, June 06, 2019	
										Sheet 29 of 57	

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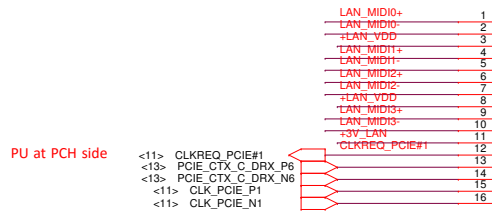
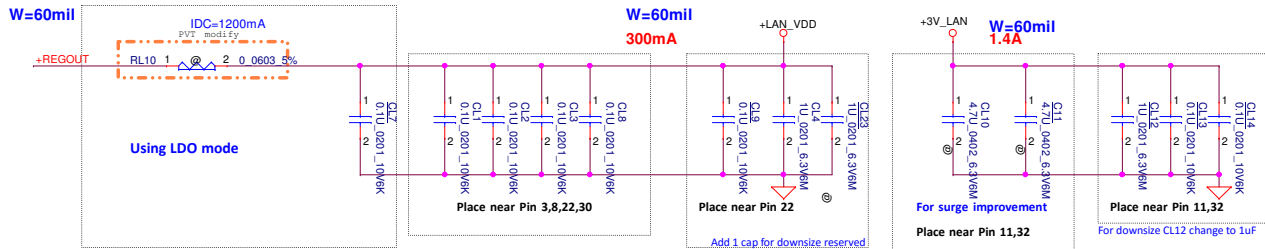
# LAN-RTL8111H



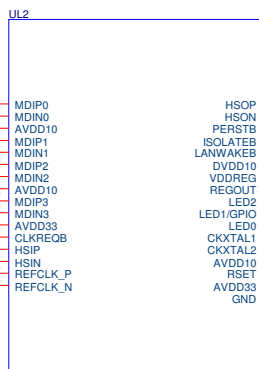
From EC

High active  
EN threshold voltage min:1.2V typ:1.6V max:2.0V  
Current limit threshold 1.5~2.8A

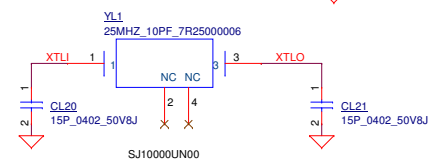
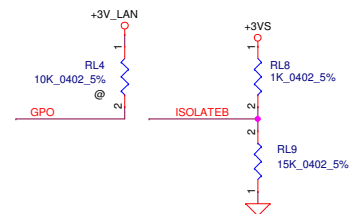
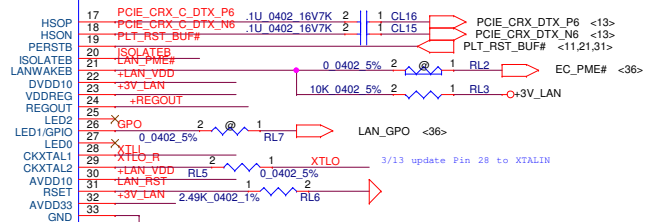
+3V\_LAN Rising time must  $>0.5\text{ ns}$  and  $<100\text{ ns}$



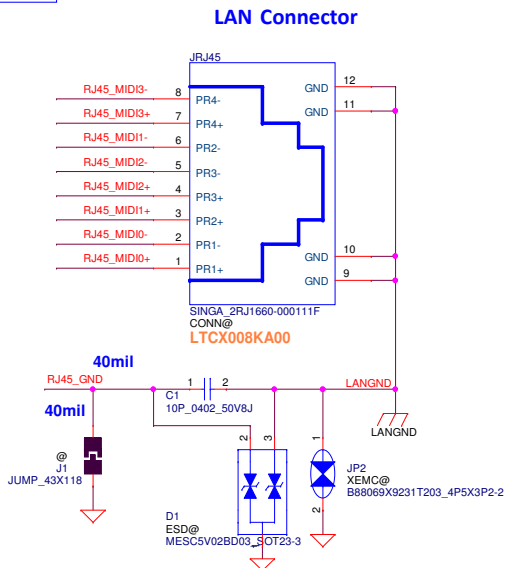
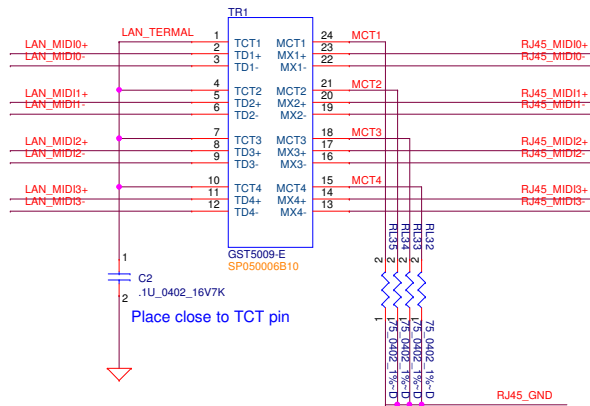
PU at PCH side



RTL8111H-CG\_QFN32\_4X4  
**SA000080P00**



12/21 change YL1 size to 20x16

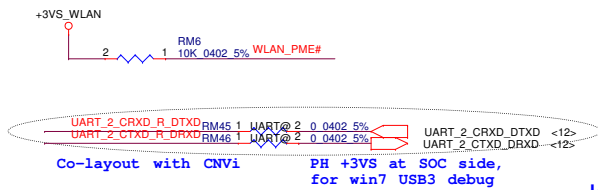


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				Customer	EHTLW M/B LA-H791P				
				Date:	Wednesday, June 19, 2019	Sheet	30	of	57

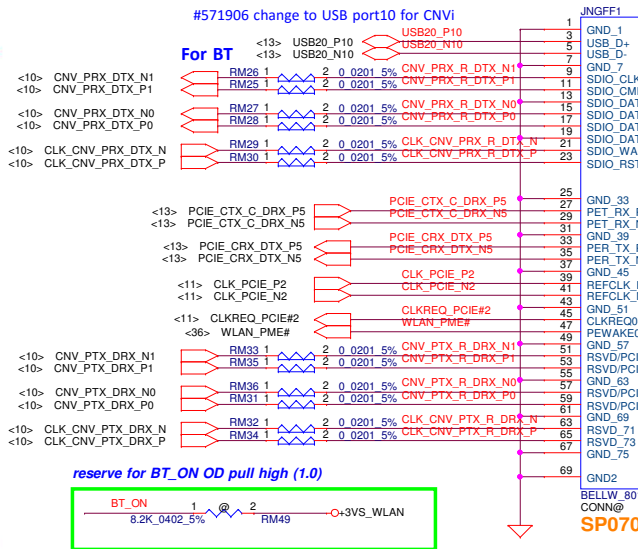
# Wireless LAN

## NGFF WL+BT (KEY E)

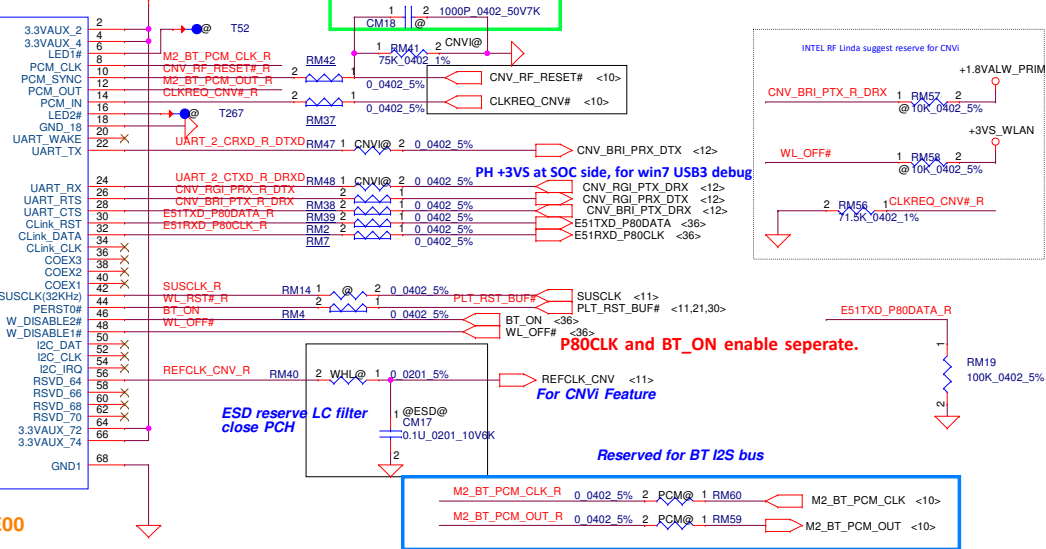
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLK_N1	73
70	UM2_Power_SRC/GPIO/PEWAKE#	RESERVED/REFCLK_P1	71
68	UM2_Power_SRC/CARDREQ#	GND	69
66	UM2_SWP/PERST#	Reserved/PER1	67
64	RESERVED	Reserved/PER1	65
62	ALERT# (IO/3.3V)	Reserved/PER1	61
60	DC CLK (IO/3.3V)	Reserved/PER1	59
58	DC DATA (IO/3.3V)	GND	57
56	W_DISABLE# (IO/3.3V)	RESERVED (IO/3.3V)	55
54	Reserved_W_DISABLE# (IO/3.3V)	CLKREQ# (IO/3.3V)	53
52	PERST# (IO/3.3V)	CLKREQ# (IO/3.3V)	51
50	SUSCLK (33MHz) (IO/3.3V)	REFCLK_N0	49
48	CODEX1 (IO/0.1V)	REFCLK_N0	47
46	CODEX2 (IO/0.1V)	REFCLK_P0	45
44	CODEX3 (IO/0.1V)	GND	43
42	VENDOR_DEFINED	PER10	41
40	VENDOR_DEFINED	GND	39
38	VENDOR_DEFINED	PER10	37
36	UART_RTS (IO/0.1V)	PER10	35
34	UART_CTS (IO/0.1V)	GND	33
32	UART_TX (IO/0.1V)	GND	31
30	UART_RX (IO/0.1V)	SDIO_RESET# (IO/0.1V)	29
28	UART_WAKE# (IO/0.1V)	SDIO_WAKE# (IO/0.1V)	27
26	GND	SDIO_DAT0 (IO/0.1V)	25
24	SDIO_DAT1 (IO/0.1V)	SDIO_DAT1 (IO/0.1V)	23
22	SDIO_DAT2 (IO/0.1V)	SDIO_DAT2 (IO/0.1V)	21
20	SDIO_DAT3 (IO/0.1V)	SDIO_DAT3 (IO/0.1V)	19
18	SDIO_DAT4 (IO/0.1V)	SDIO_DAT4 (IO/0.1V)	17
16	SDIO_DAT5 (IO/0.1V)	SDIO_DAT5 (IO/0.1V)	15
14	SDIO_DAT6 (IO/0.1V)	SDIO_DAT6 (IO/0.1V)	13
12	SDIO_DAT7 (IO/0.1V)	SDIO_DAT7 (IO/0.1V)	11
10	SDIO_DAT8 (IO/0.1V)	SDIO_DAT8 (IO/0.1V)	9
8	SDIO_DAT9 (IO/0.1V)	SDIO_DAT9 (IO/0.1V)	7
6	SDIO_DAT10 (IO/0.1V)	SDIO_DAT10 (IO/0.1V)	5
4	SDIO_DAT11 (IO/0.1V)	SDIO_DAT11 (IO/0.1V)	3
2	SDIO_DAT12 (IO/0.1V)	SDIO_DAT12 (IO/0.1V)	1



## KEY E

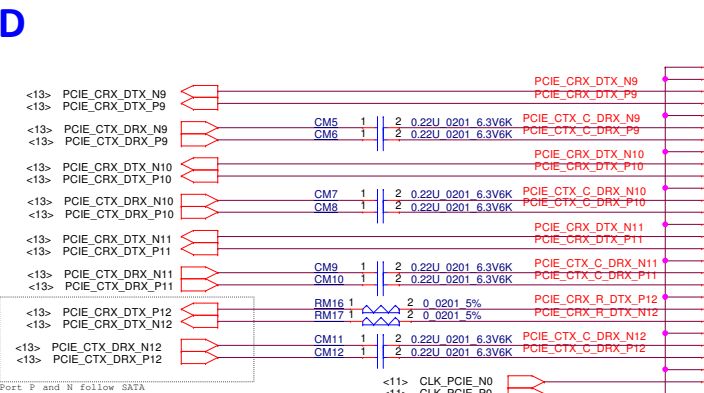


## KEY E



## mSATA/SSD

PETp0/SATA-A+	49
PETn0/SATA-A-	47
GND	45
PERp0/SATA-B-	43
PERn0/SATA-B+	41



## KEY M

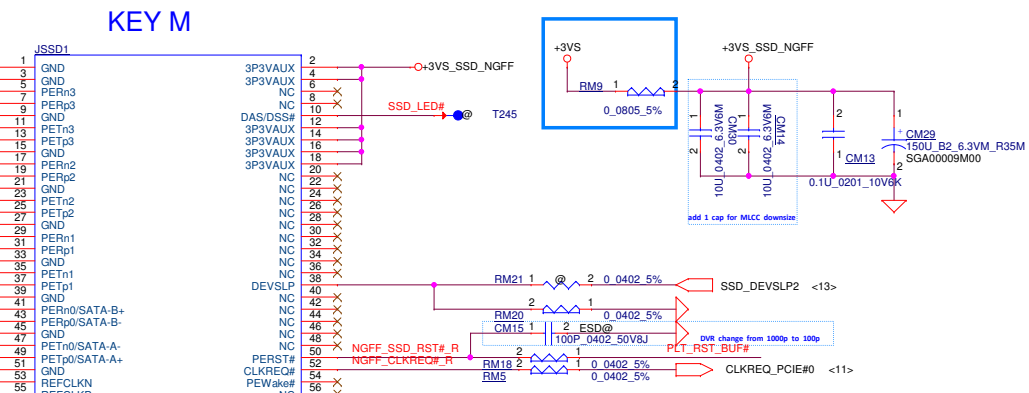
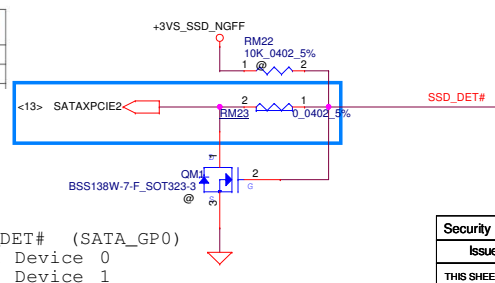


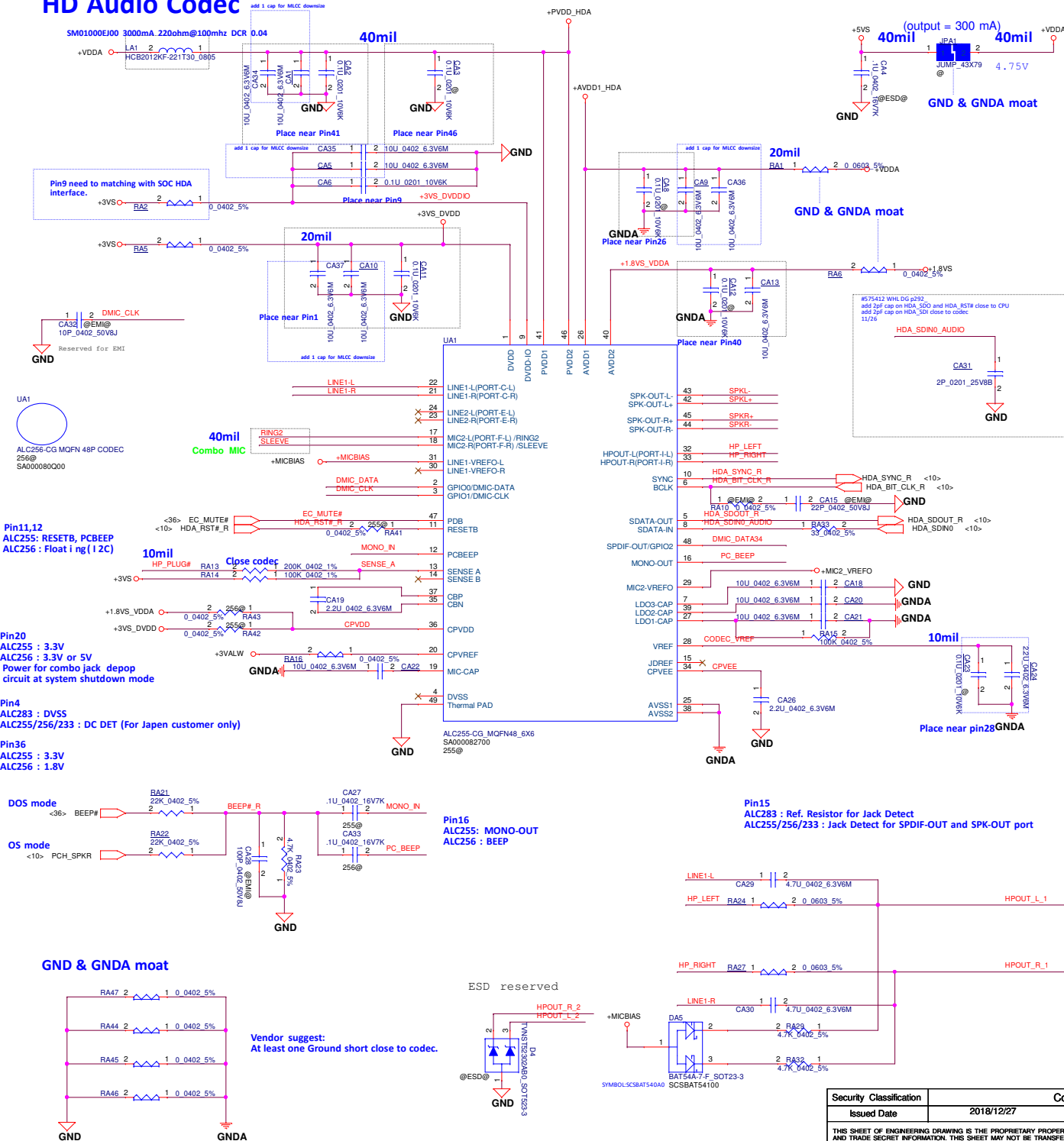
Table 35-7. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF	None	None

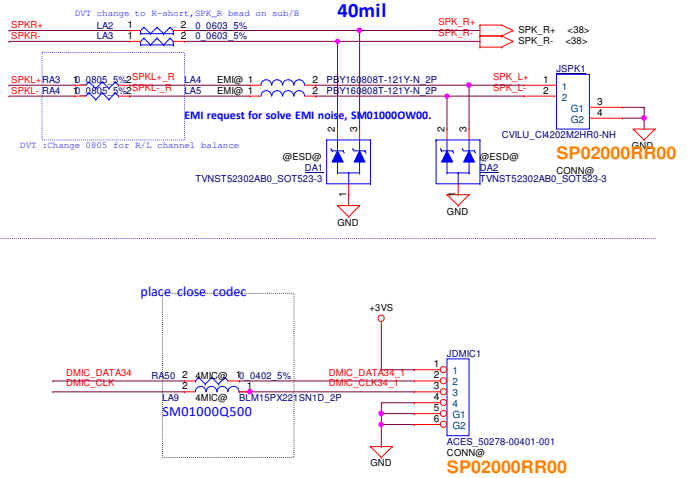


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				Date	Thursday, June 06, 2019
				Sheet	31 of 57

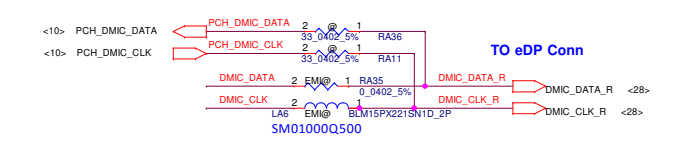
# HD Audio Codec



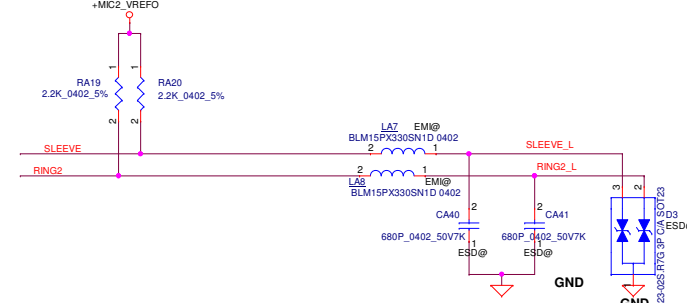
## Int. Speaker Conn.



## Digital MIC

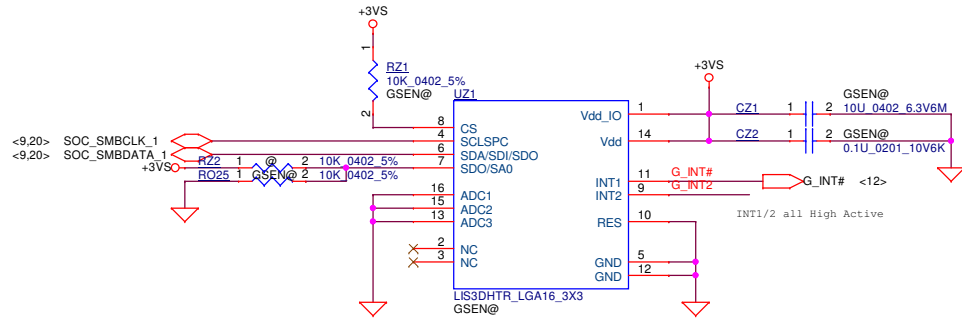


## Headphone Out

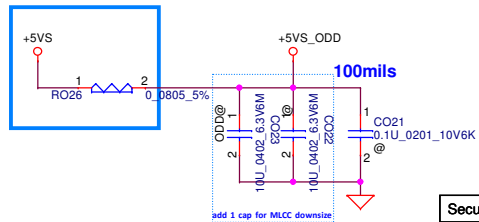
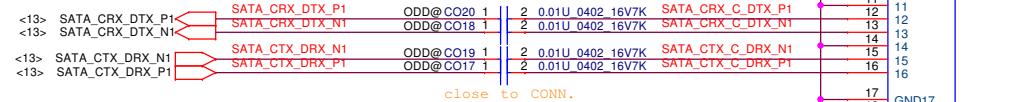
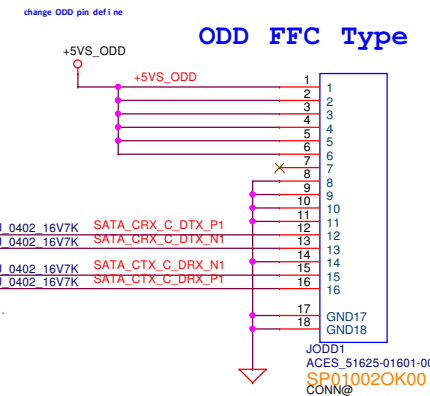
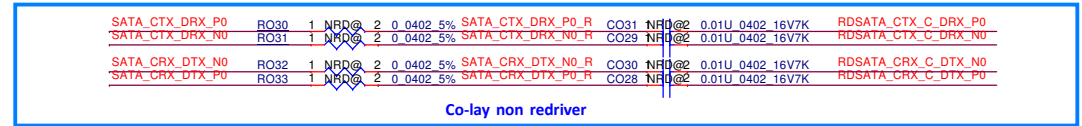
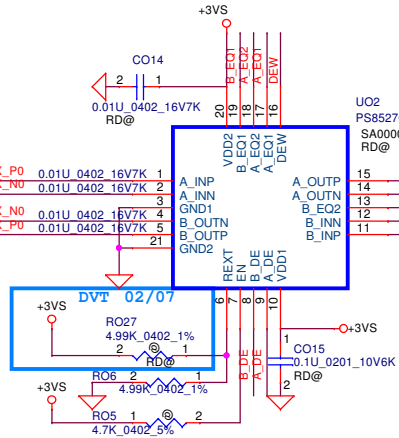
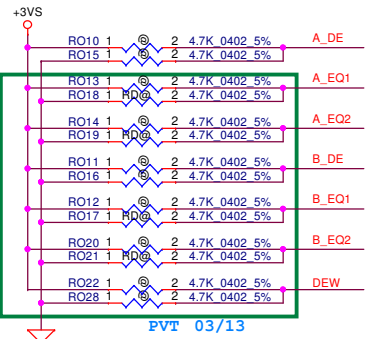
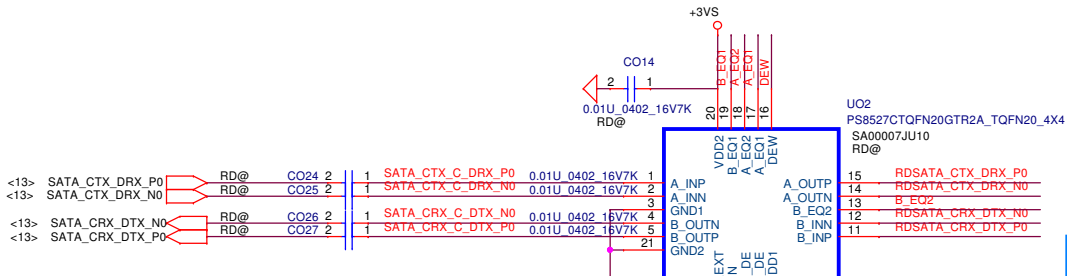
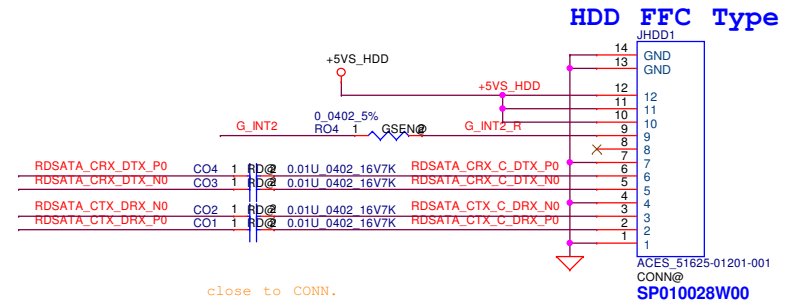
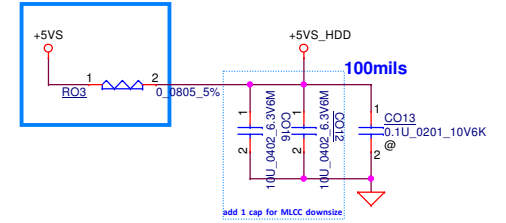
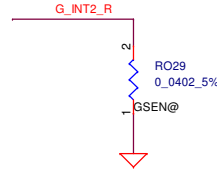


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		Customer		EH7LW/MB LA-H791P	
		Date:		Thursday, June 06, 2019	
		Sheet		32 of 57	

## G-Sensor reserved for BA serial



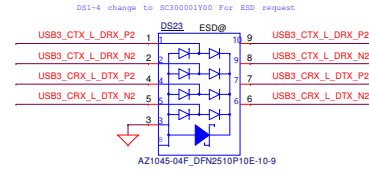
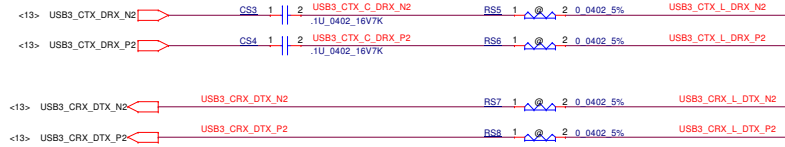
```
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)
```



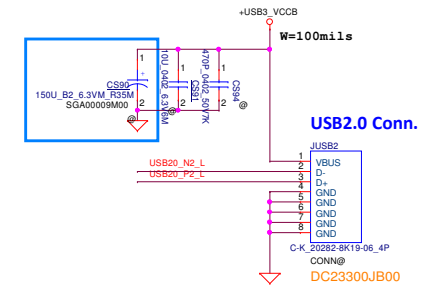
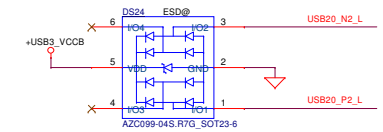
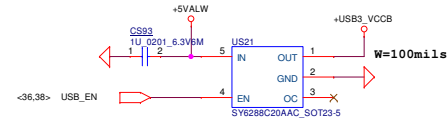
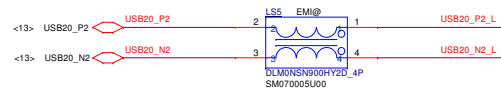
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
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				Size	Document Number
				Custort	rev
				EH7LW M/B LA-H791P	
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## USB3.0 (Port 2)

USB3 port reserved



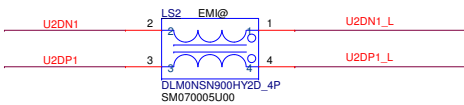
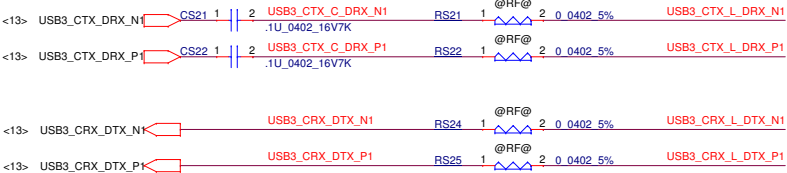
## USB2.0 (Port 2)



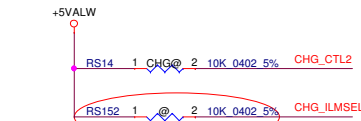
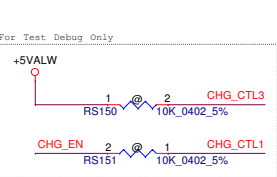
Symbol: DC23300N800  
compatible: DC23300TT00

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				Custom	EH7LW M/B LA-H791P
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				Rev	0.2

USB3.0 (Port 1)



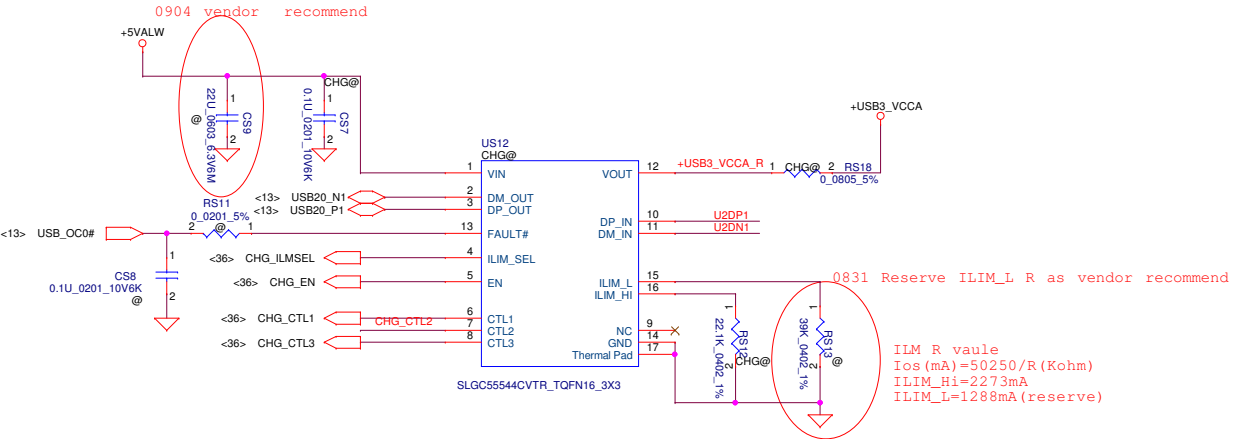
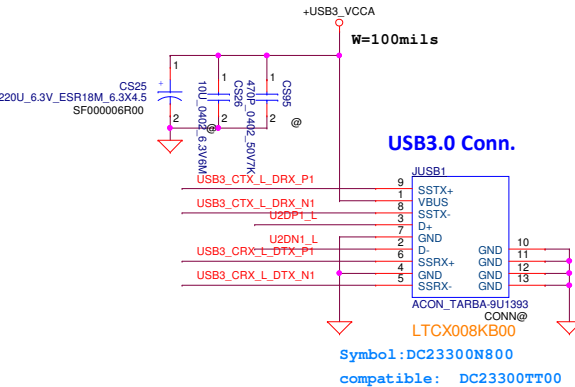
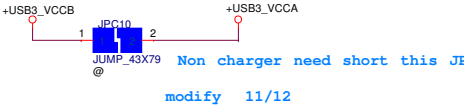
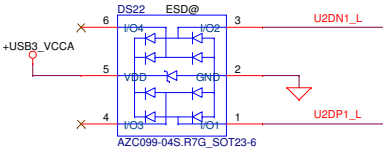
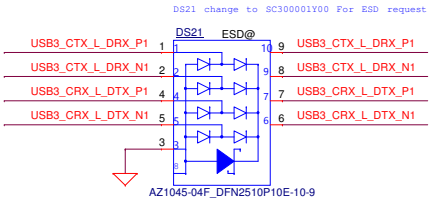
DVT: R-short



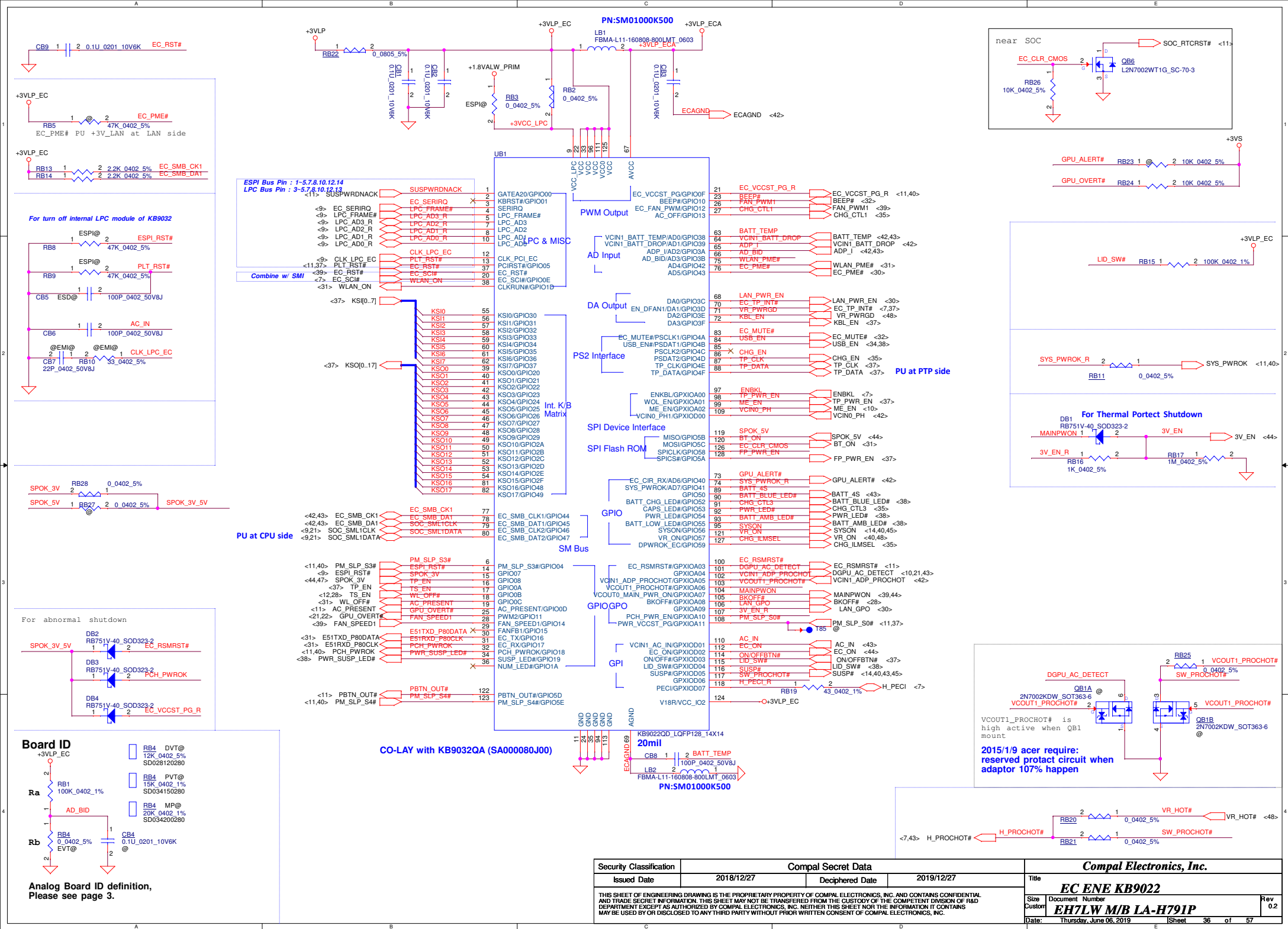
Reserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected



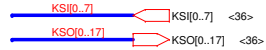
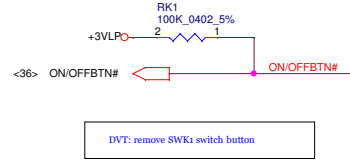




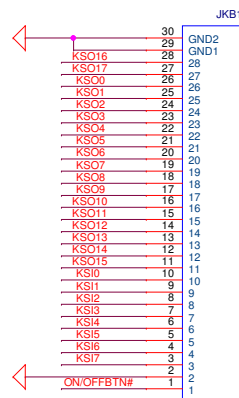
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>			
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	<b>EC ENE KB9022</b>		
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				Custor	<b>EH7LW M/B LA-H791P</b>	0.2	
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## ON/OFF BTN

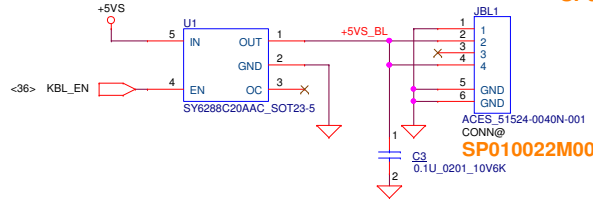


## KB Conn.



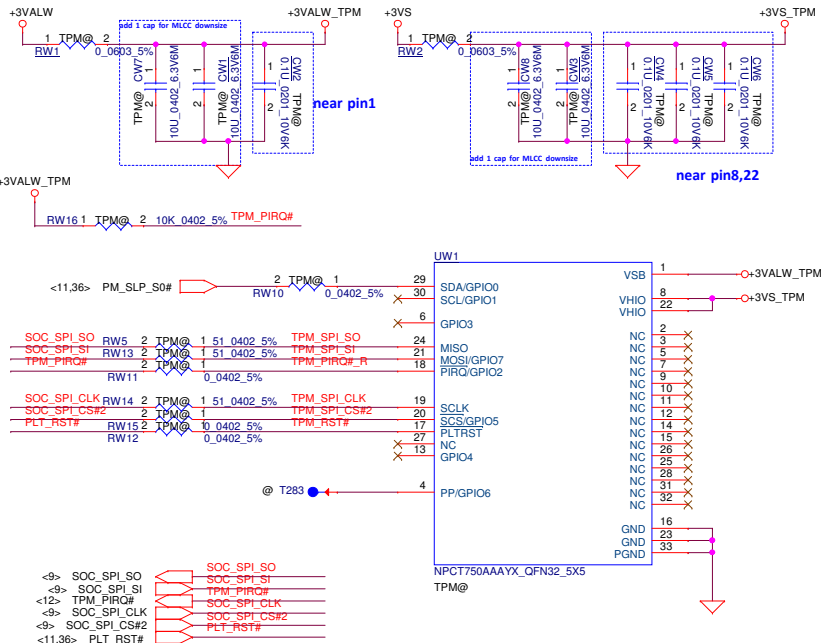
ACES\_85201-2805  
CONN@  
SP01000GO00

## KB BackLight



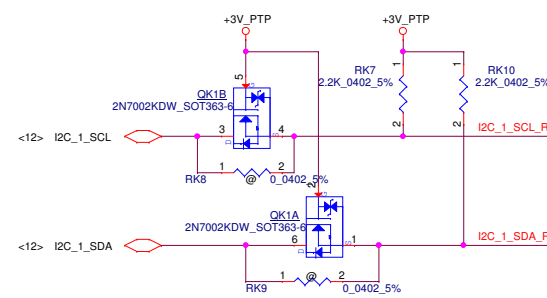
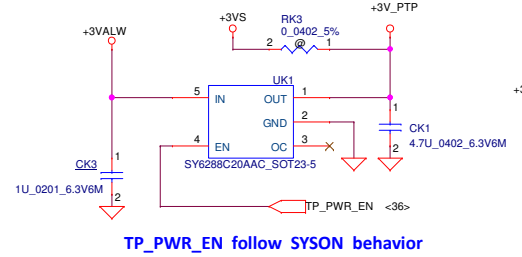
ACES\_51524-0040N-001  
CONN@  
SP010022M00

## TPM 2.0

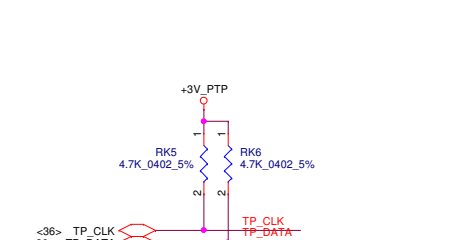
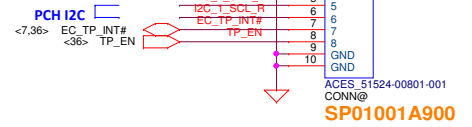


SA0000AQ230, 5 IC NPCT750AAAYX QFN 32P TPM (SPI interface)

## TP/B Conn.

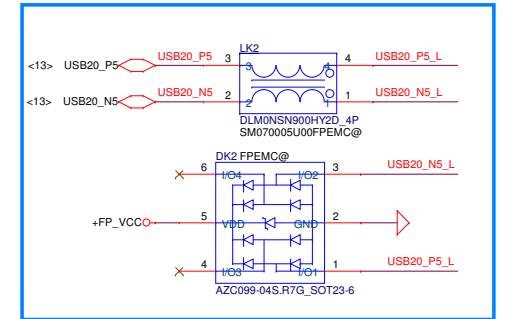
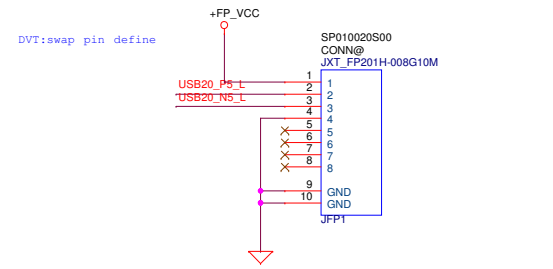
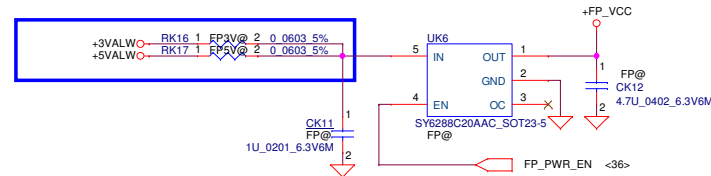


## EC PS2



## Finger Print

Power Souce Check  
EGIS ETU801 +FP\_VCC=5V  
ELAN SA464K-2200 +FP\_VCC=3.3V



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Issued Date		2018/12/27		Deciphered Date		2019/12/27		Title			
								KB & TP & TPM & FP			
Size		Document		Number		Rev		EH7LW MB LA-H791P			
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## USB I/O



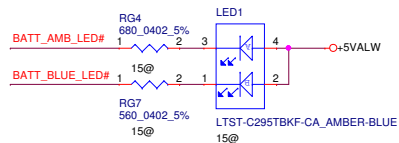
Reserved CMC on SUB/B side

## Card reader

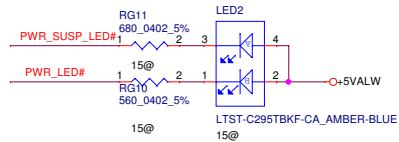


## LED for 15" UMA

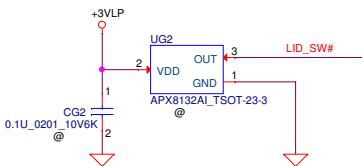
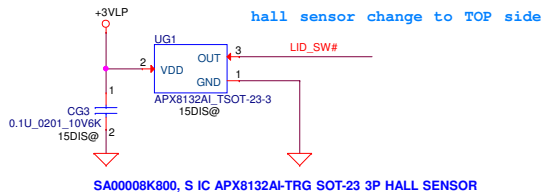
### Battery LED



### Power LED

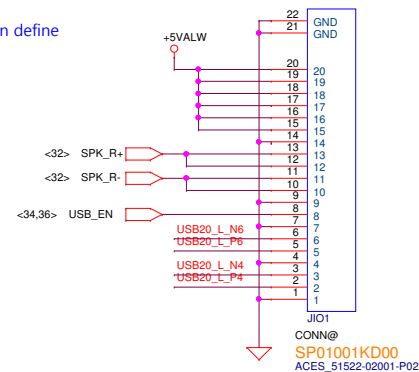


## LID for 15" DIS

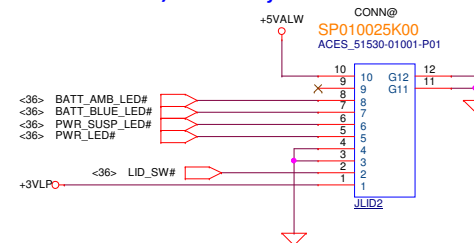


## I/O Borad (USB2 /Card reader/ Speaker-RCH)

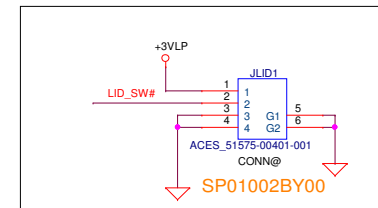
DVT:update JIO1 pin define



## LID/B with LED for 17" UMA &DIS

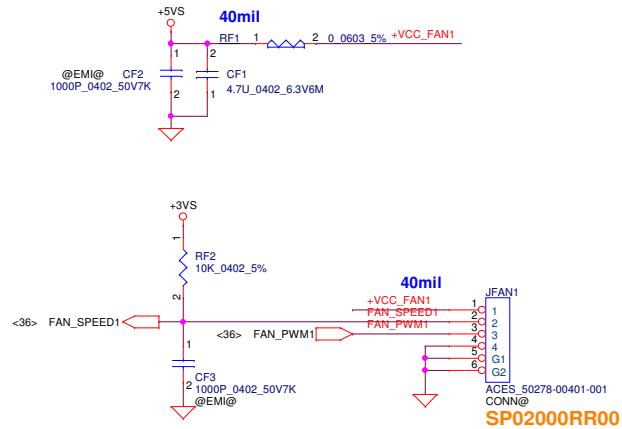


## LID/B for 15" UMA 4pin

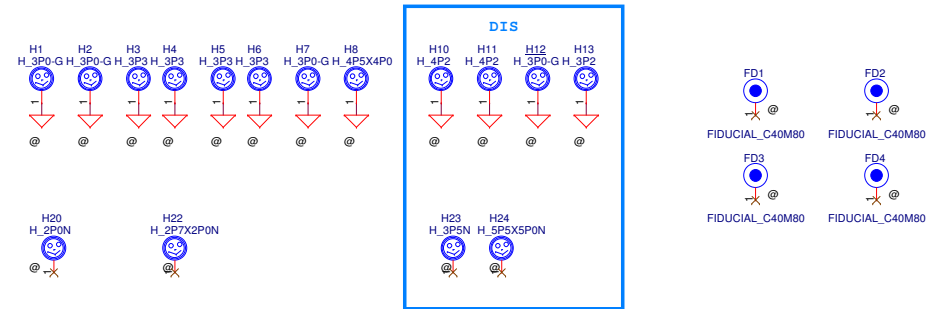


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Issued Date				2018/12/27		Deciphered Date		2019/12/27		Title	
										IO/LID/LED	
										Size Document Number	
										EH7LW M/B LA-H791P	
										Rev 0.2	
										Date: Thursday, June 06, 2019	
										Sheet 38 of 57	

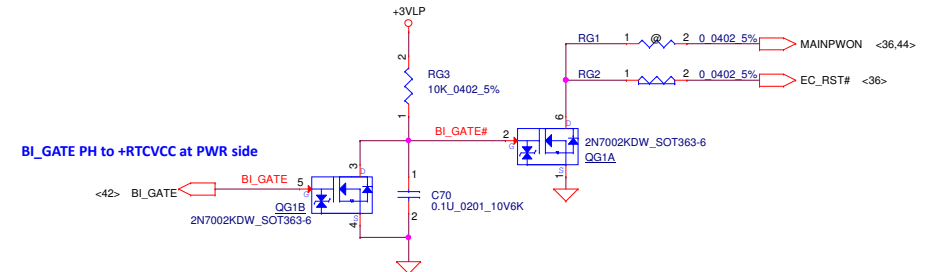
## FAN1 Conn



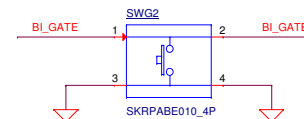
## Screw Hole



## Reset Circuit

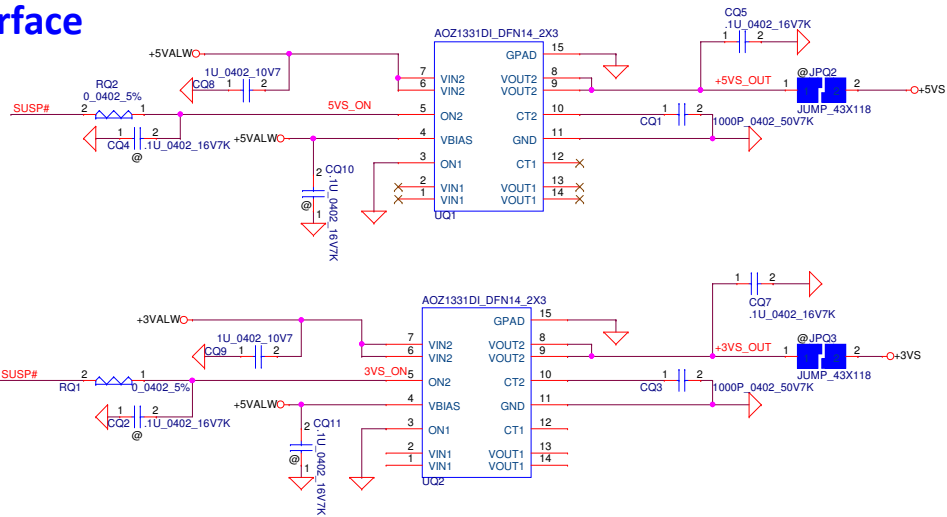


## Reset Button

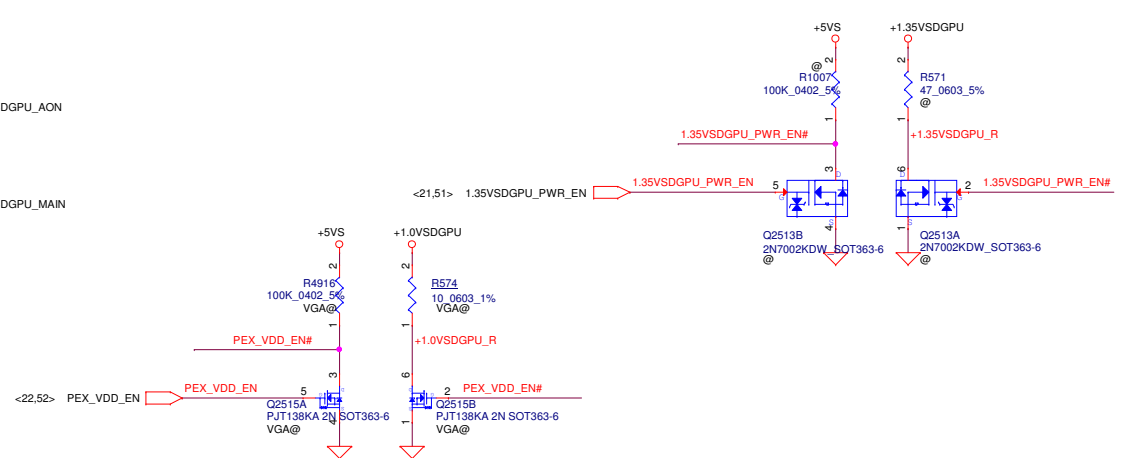
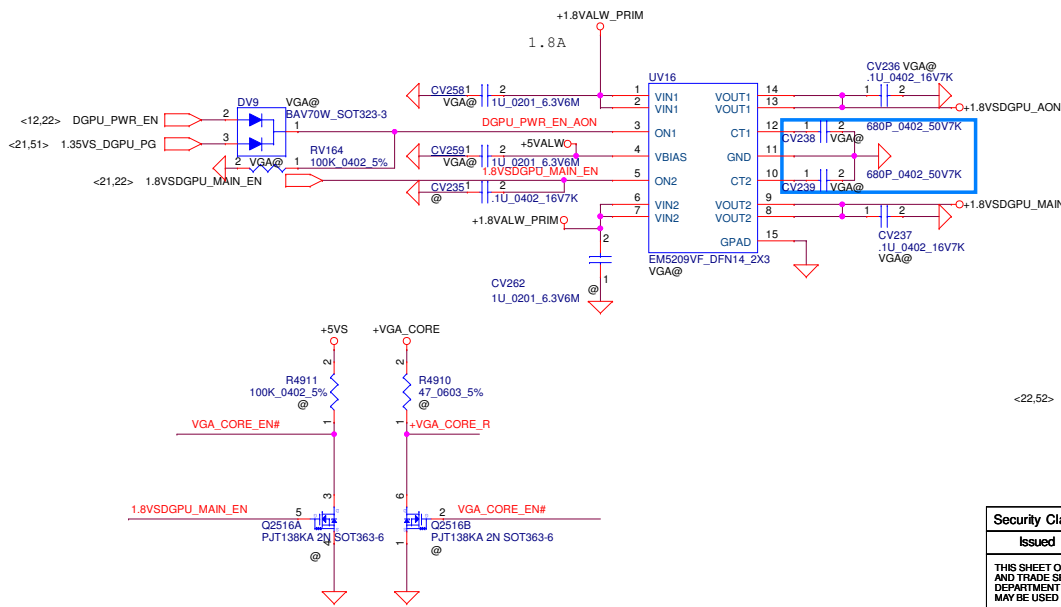
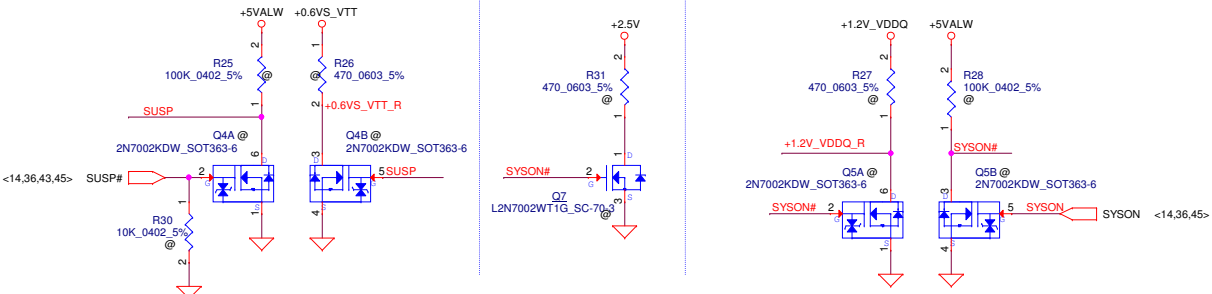
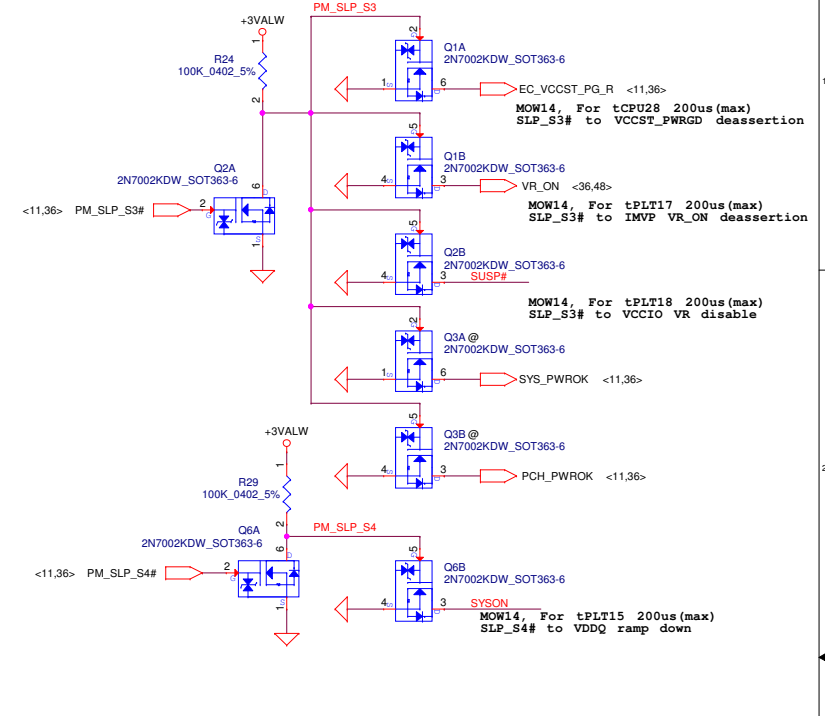


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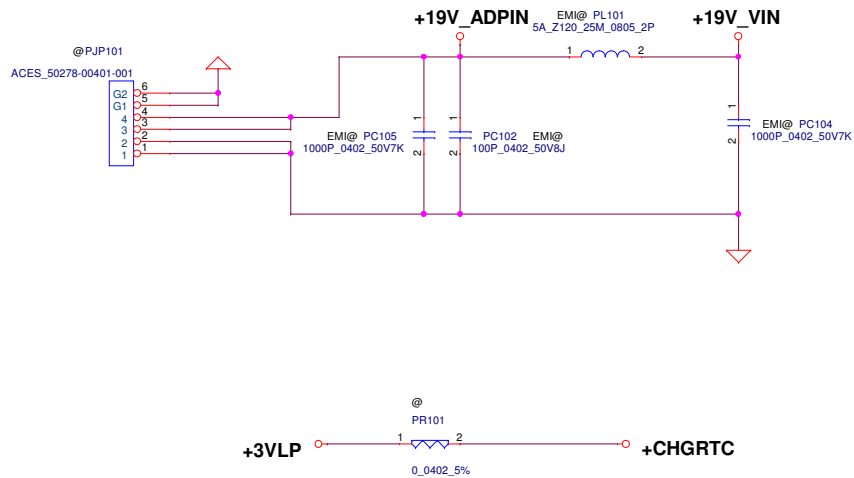
## DC Interface



## For Power ON/Off Sequence



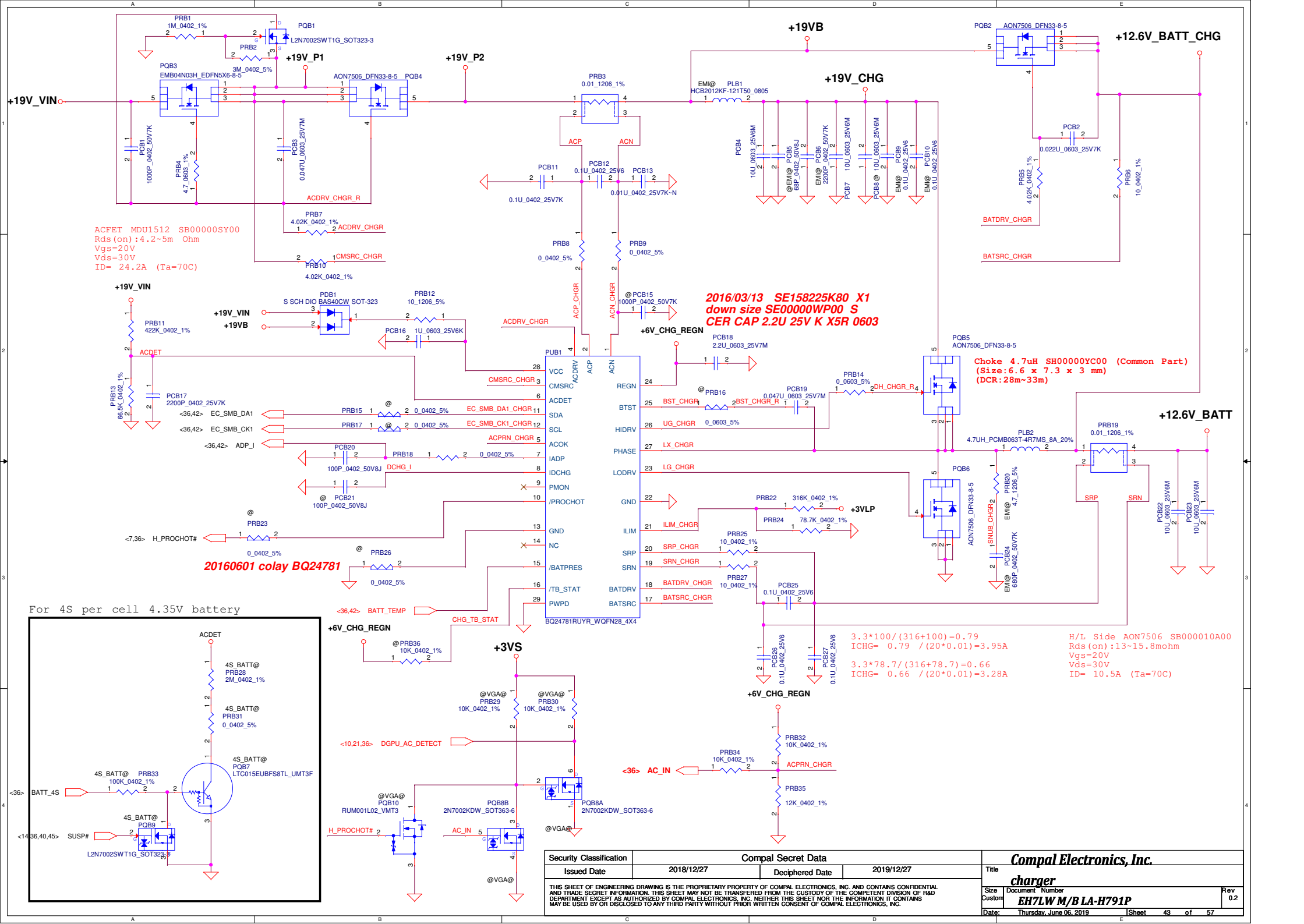
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Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
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				Custom	Rev
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				PWR DCIN / Pre-charge			
				Size			
				Document Number		Rev	
				EH7LW M/B LA-H791P		0.2	
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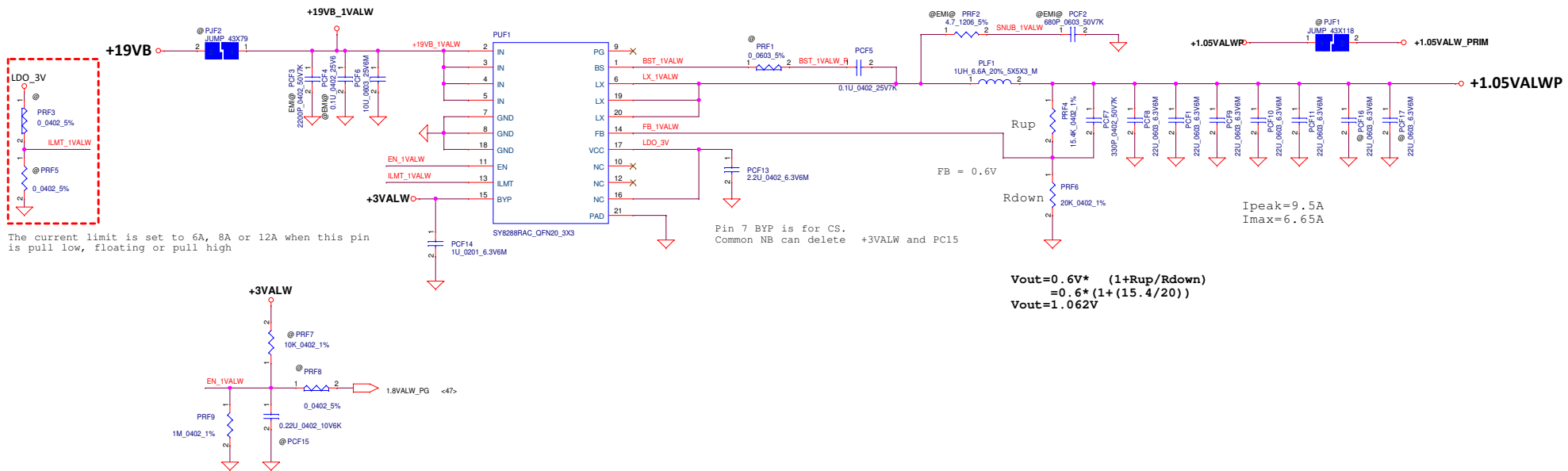




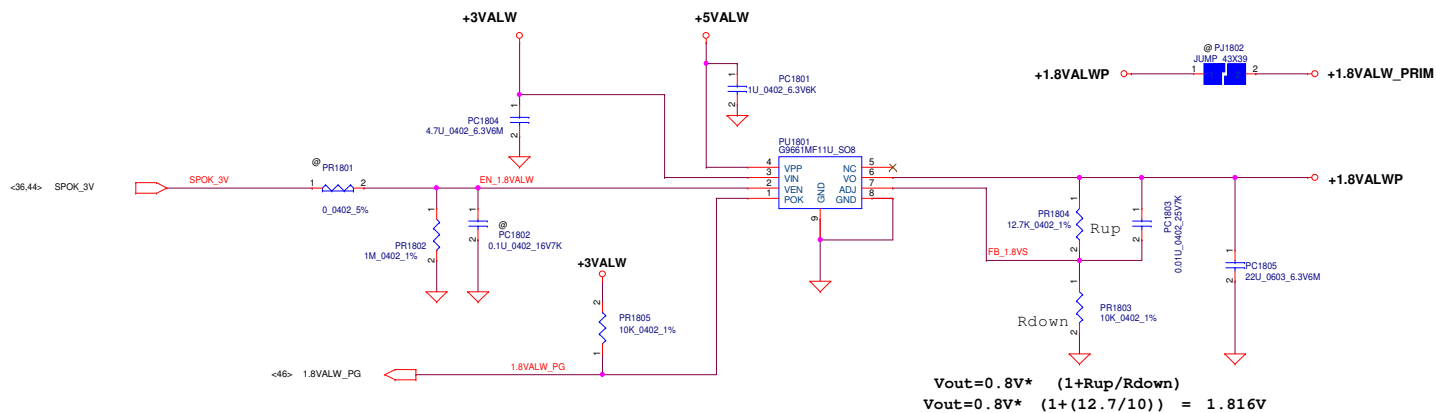




EN pin don't floating  
If have pull down resistor at HW side, pls delete PR702

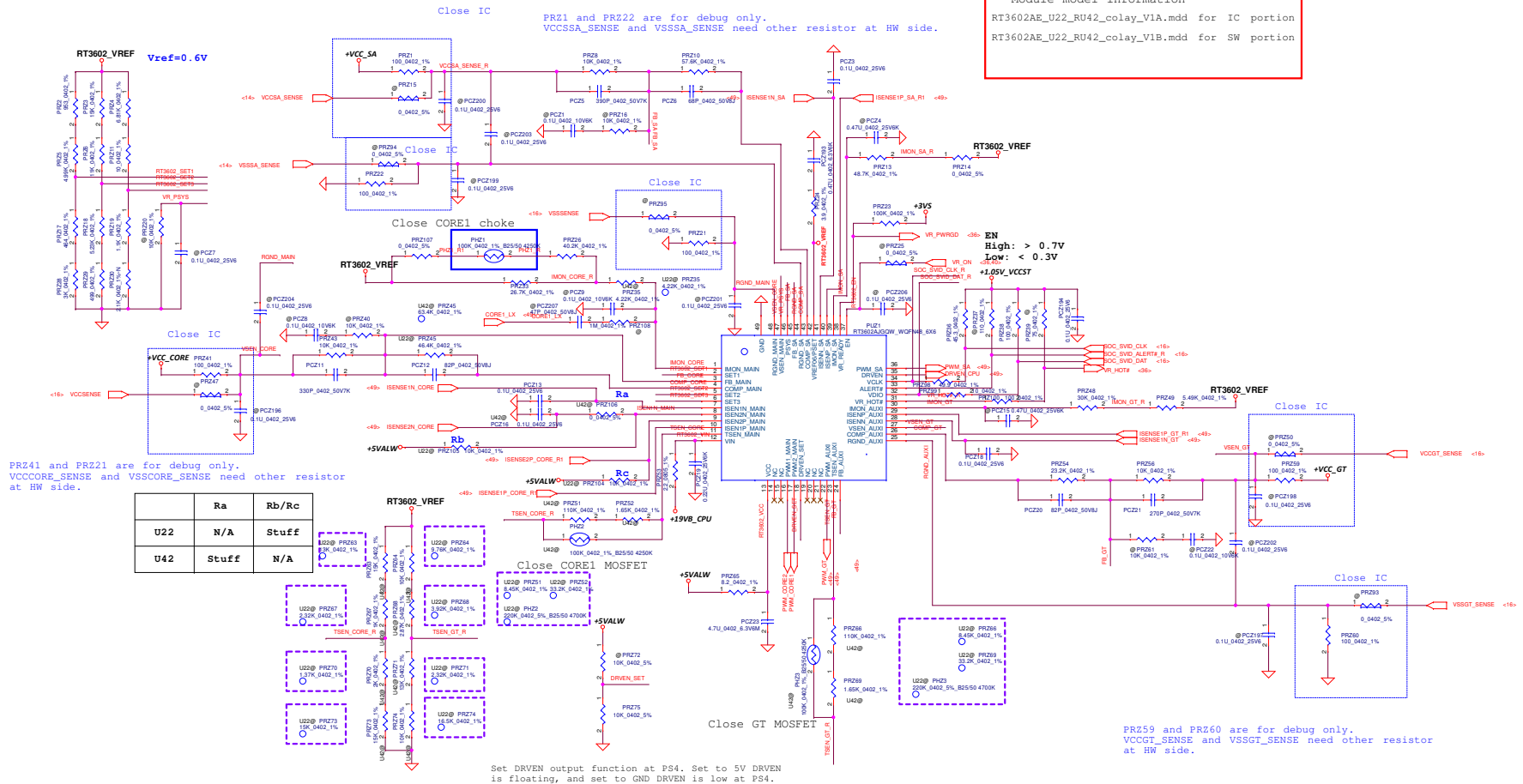


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				C	EH7LW M/B LA-H791P
				Date:	Thursday, June 06, 2019
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Module model information  
RT3602AE\_U22\_RU42\_colay\_V1A.mdd for IC portion  
RT3602AE\_U22\_RU42\_colay\_V1B.mdd for SW portion

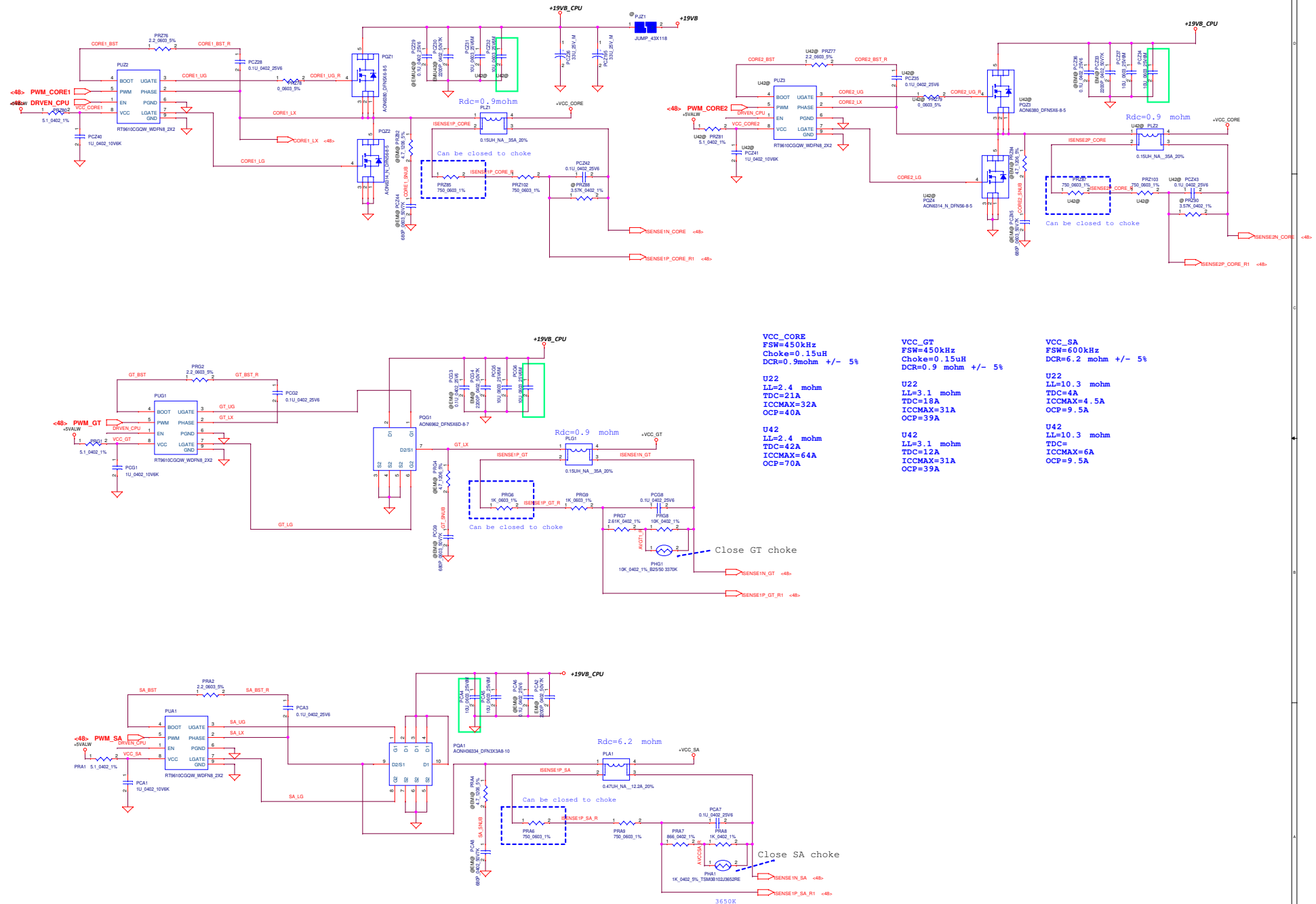


PRZ41 and PRZ21 are for debug only.  
VCCCORE\_SENSE and VSSCORE\_SENSE need other resistor at HW side.

	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

PRZ59 and PRZ60 are for debug only.  
VCCGT\_SENSE and VSSGT\_SENSE need other resistor at HW side.





VCC\_CORE  
FSW=450kHz  
Choke=0.15uH  
DCR=0.9mohm +/- 5%

VCC\_GT  
FSW=450kHz  
Choke=0.15uH  
DCR=0.9mohm +/- 5%

VCC\_SA  
FSW=600kHz  
DCR=6.2mohm +/- 5%

U22  
LI=2.4mohm  
TDC=21A  
ICCMAX=32A  
OCP=40A

U22  
LI=3.1mohm  
TDC=19A  
ICCMAX=31A  
OCP=39A

U22  
LI=10.3mohm  
TDC=4A  
ICCMAX=4.5A  
OCP=9.5A

U42  
LI=2.4mohm  
TDC=42A  
ICCMAX=64A  
OCP=70A

U42  
LI=3.1mohm  
TDC=12A  
ICCMAX=31A  
OCP=39A

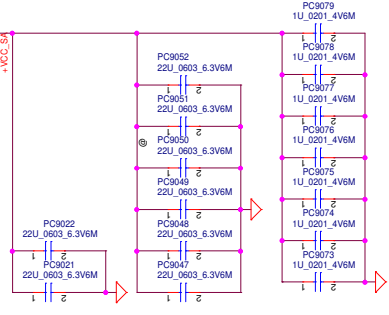
U42  
LI=10.3mohm  
TDC=6A  
ICCMAX=6A  
OCP=9.5A

Close GT choke

Close SA choke

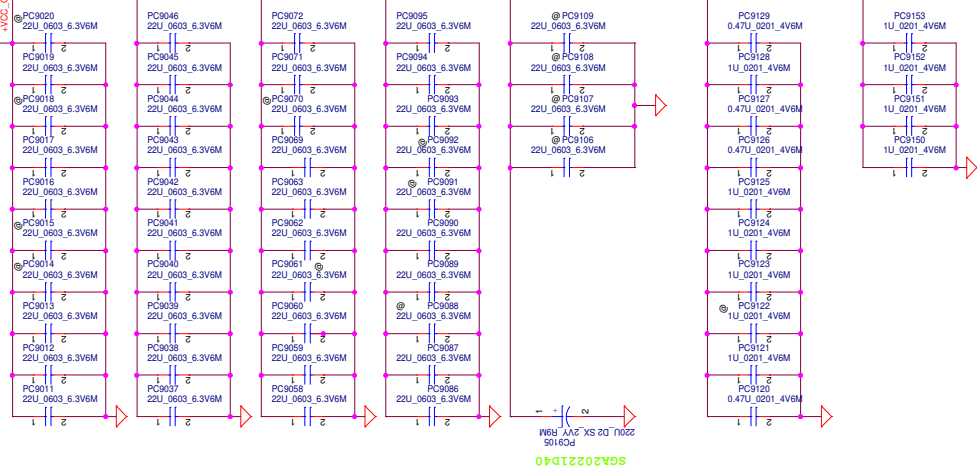
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	CPU Power stage
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+VCC\_SA



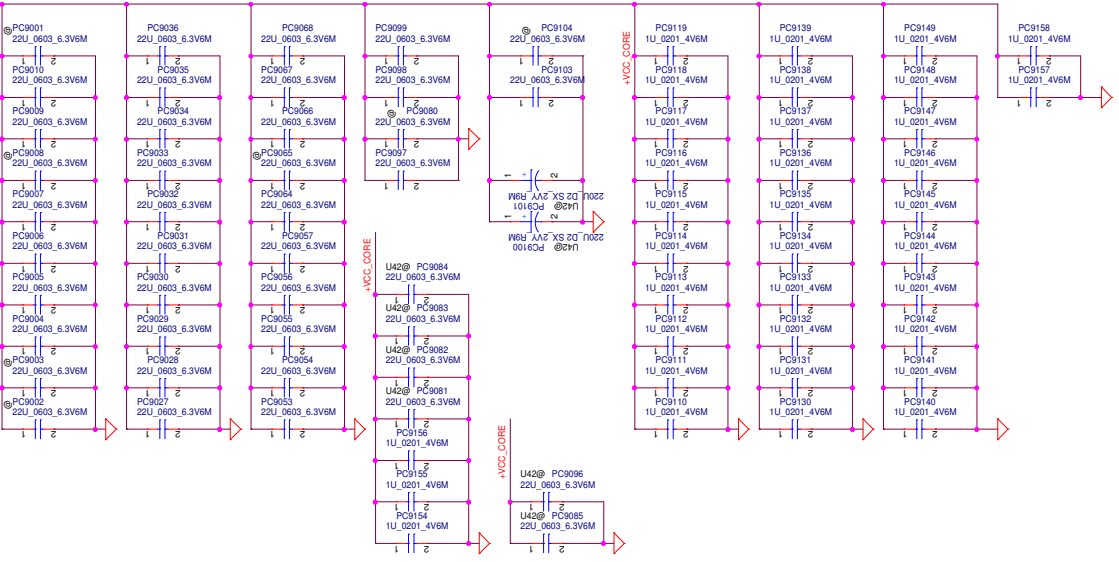
SA  
pop: 22uF\_0603\*7  
22uF\*31  
1uF\*9  
unpop: 1uF\_0201\*7  
22uF\_0603\*1

+VCC\_G7



220uF\*1  
22uF\*31  
1uF\*9  
0.47uF\*4  
unpop: \*13  
22uF \*1

+VCC\_CORE

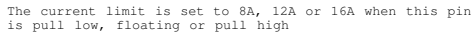


2017/07/03  
VCORE Output Capacitor:  
U42  
22uF\_0603\*35  
1uF\_0201\*35  
220uF \*2  
UNPOP  
22\_0603\*7  
220uF \*2

2017/07/03  
VCORE Output Capacitor:  
U22  
22uF\_0603\*29  
1uF\_0201\*35  
UNPOP  
22\_0603\*7  
220uF \*2

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				Power Train	
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<21,40> 1.35VS\_DGPU\_PG

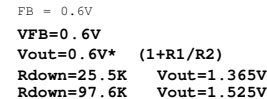


		GPU Core	GPU FBIO		FB Total <sup>1, 5</sup>		1.05V Total <sup>2</sup>	3.3V Total
		—	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.05V <sup>4</sup>	3.3V <sup>4</sup>
Products	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)	
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GXR	GDDR5	35.4	—	2.4	—	4.9	2.6	0.40

		GPU Core	GPU FBIO		FB Total <sup>1,5</sup>		1.05V Total <sup>2</sup>
		—	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.05V <sup>4</sup>
Products	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1
N16S-GXR	GDDR5	54.0	—	4.6	—	9.5	2.9

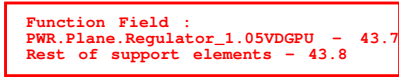
	NVVD	GPU FBIO	FB Total <sup>5</sup>	1.0V Total <sup>1</sup>	1.8V Total <sup>2</sup>
	—	1.35V <sup>4</sup>	1.35V <sup>4</sup>	1.0V <sup>4</sup>	1.8V <sup>4</sup>
Product	(A)	(A)	(A)	(A)	(A)
N175-G1	29.7	2.0	3.4	0.1	0.3
N175-LG	15.4	1.6	2.8	0.1	0.2

	NVVD	GPU FBIO	FB TOTAL <sup>4</sup>	1.0V Total <sup>1</sup>
Product <sup>2</sup>	—	1.35V <sup>3</sup>	1.35V <sup>3</sup>	1.0V <sup>3</sup>
	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2



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Module model information
SY8032_V2.mdd
```



$V_{out} = 0.6V * (1 + R_{up}/R_{down})$   
 $N16 > 1.05V$   
 $=> 0.6V * (1 + (7.68/10)) = 1.061$  (1.01%)  
 $=> 0.6V * (1 + (7.32/10)) = 1.039$  (-1%)  
 $N17 > 1.0V$   
 $V_{out} = 0.6V * (1 + (6.98/10)) = 1.019V$  (1.02%)

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R1, R2, R3, R4, R5, C are based on VGA type to set.

R1  
N16S\_VGA@ PR1209  
20K\_0402\_1%

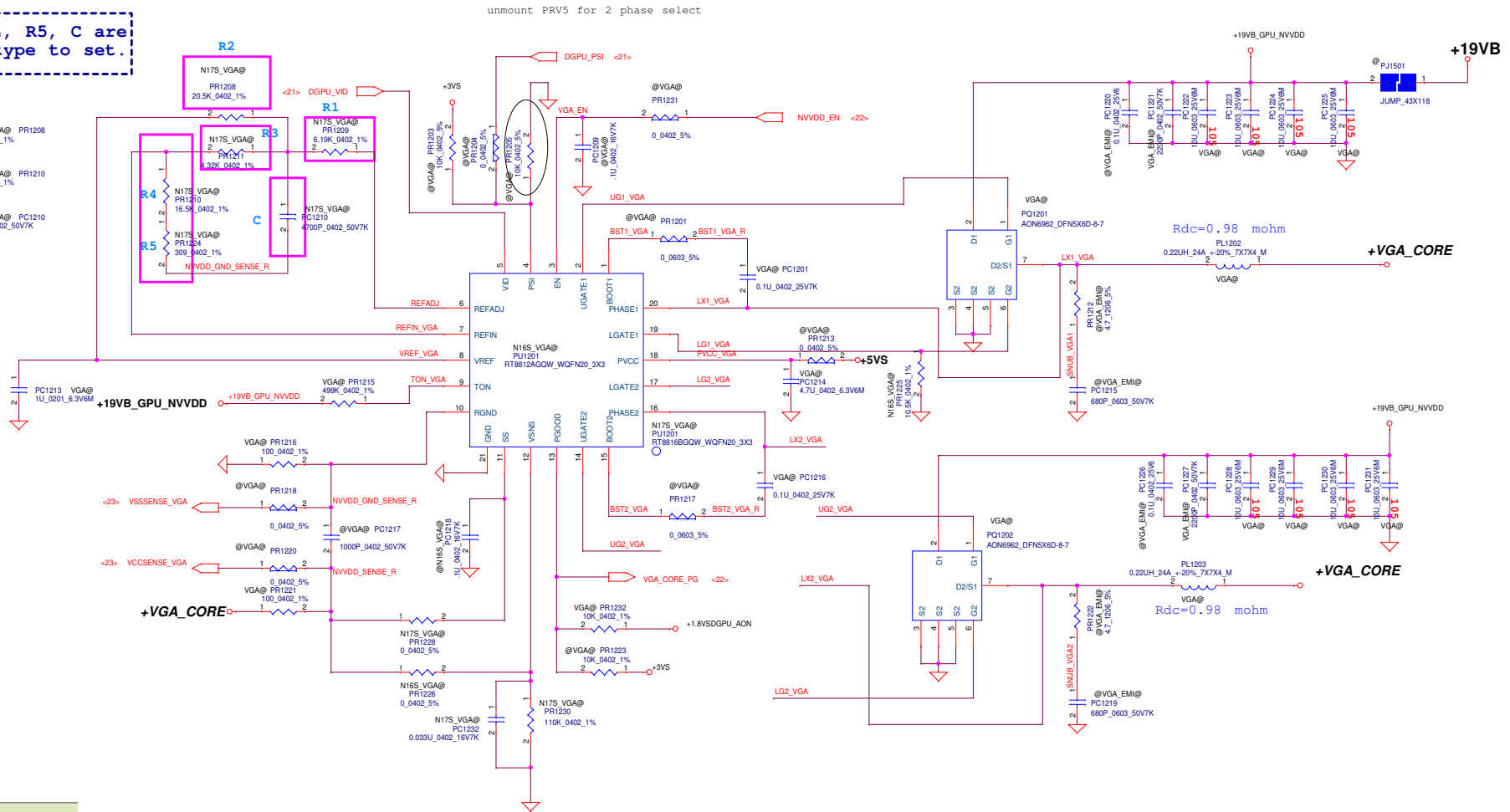
R2  
N16S\_VGA@ PR1208  
20K\_0402\_1%

R3  
N16S\_VGA@ PR1211  
2K\_0402\_1%

R4  
N16S\_VGA@ PR1210  
10K\_0402\_1%

R5  
N16S\_VGA@ PR1224  
0.0402\_5%

C  
N16S\_VGA@ PC1210  
2700P\_0402\_50V7K



PWM-VID Specification		
		Config B
Vmin	V	0.6
Vmax	V	1.2
Vboot	V	0.9
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	96
PWM Frequency F <sub>PWM</sub>	MHz	1.125
PWM Minimum Pulse Width T <sub>DMIN</sub>	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	20
R2 (1%)	KΩ	20
R3 (1%)	KΩ	2
R4 (1%)	KΩ	18
R5 (1%)	KΩ	0
C	nF	2.7

N17x DG-07875-001\_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F <sub>PWM</sub>	kHz	675
PWM Minimum Pulse Width T <sub>DMIN</sub>	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Table 6. EDP-Continuous<sup>3</sup>

Products	VRAM Type	GPU Core
N16S-GMR	GDDR5	19.0
	DDR3/L	21.0
N16S-GTR	GDDR5 @ 2.0 GHz	26.5
	GDDR5 @ 2.5 GHz	26.5
	DDR3/L	26.0
N16S-GXR	GDDR5	35.4

Table 7. EDP-Peak<sup>3</sup>

Products	VRAM Type	GPU Core
N16S-GMR	GDDR5	34.0
	DDR3/L	39.5
N16S-GTR	GDDR5 @ 2.0 GHz	53.0
	GDDR5 @ 2.5 GHz	53.0
	DDR3/L	51.0
N16S-GXR	GDDR5	54.0

Table 7. Output EDP-Continuous

	NVDD	GPU FBIO	FB Total <sup>3</sup>	1.0V Total <sup>1</sup>	1.8V Total <sup>2</sup>
	—	1.35V <sup>4</sup>	1.35V <sup>4</sup>	1.0V <sup>4</sup>	1.8V <sup>4</sup>
Product	(A)	(A)	(A)	(A)	(A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

	NVDD	GPU FBIO	FB TOTAL <sup>4</sup>	1.0V Total <sup>1</sup>
	—	1.35V <sup>3</sup>	1.35V <sup>3</sup>	1.0V <sup>3</sup>
Product	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Reserve gpu prochot function	Reserve gpu prochot function		P.43	Del PQB8 for function reserve.	19.0103	EVT
02	change PL502 to common part	change PL502 to common part		P.44	change PL502 to common part(SH000016700)	19.0212	DVT
03	change PR1230 to 110K	change PR1230 to 110K for ocp setting		P.53	change PR1230 to 110K(SD034110380)	19.0212	DVT
04	change CAP size to 0402	change CAP size to 0402 for cost down		P.43,44	change PC302,PC502,PCB11 to SE00000W210 change PCB1 to SE074102K80	19.0212	DVT
05	change 0 ohm to R-short	change 0 ohm to R-short for cost down			change PR101,PR217,PR210,PRB15,PRB17,PRB23,PRB26,PRB16,PR304,PR505,PR502,PRM8,PRM11,PRM12,PRF3,PRF8,PRF1,PR1801,PRZ15,PRZ94,PRZ47,PRZ95,PRZ50,PRZ93,PRZ25,PRW5,PRW9,PRW6,PRW1,PRW3,PRE5,PR1231,PR1204,PR1218,PR1220,PR1201,PR1217,PR1213 to R-short (38PCS)	19.0212	DVT
06	DDR sequence	change PRM8 to 48.7K and PCM18 to 0.1u for sequence		P.38	change PRM8 to SD034487280 change PCM18 to SE102104K00	19.0215	DVT
07	CPU transient	change R and C value for CPU transient test		P.48	change PCZ11 to 330PuF(SE074331K80) change PRZ45 to 63.4k ohm(SD03463K280)(U42) change PRZ49 to 5.49k ohm(SD034549180)	19.0218	DVT
08	DDR sequence	change PRM8 to 0 ohm and del PCM18 for sequence		P.38	change PRM8 to SD028000080 del PCM18	19.0328	PVT
09	VR thermal alert adjust	change protect from 100c to 110c		P.48	change PHZ2,PHZ3 to SL200002I00, change PRZ51,PRZ66 to SD000000680, change PRZ52,PRZ69 to SD034332280, change PRZ67 to SD00000WS80,change PRZ63 to SD034130280, change PRZ70 to SD034137180,change PRZ68 to SD0343392180, change PRZ64 to SD034976180,change PRZ71 to SD00000WS80,change PRZ74 to SD034165280	19.0507	pre MP
10							
11							
12							
13							
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15							
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18							
19							

HW Schematic chang list (P.I.R)

Date	Rev.	Modify Item	Date	Rev.	Modify Item
1/25	0.2	Add cnvi cap(CM4) as intel request Swap JFP1 pin define update JI01 pin define update H12 hole,downsize C2034/C2750			
1/29	0.2	update JI01 pin define change 0-ohm to R-short remove SWK1			
2/12	0.2	change RA3/RA4 to 0805 size			
3/13	1A	update UL2 pin28/pin29 pin define Add DA3/DA4 for audio ESD protection update JI01 footprint			
5/9	1B	update RC262 75k for CML			

HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
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